

# Watchmen/Cyborg AMD Schematics Lucienne

2021-01-18

REV : A00

*DY : None Installed*

*UMA: UMA only installed*

*OPS: DISCRTE OPTIMUS installed*

<Core Design>



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Title

**Cover Page**

Size  
A3

Document Number

**Watchmen/Cyborg AMD**

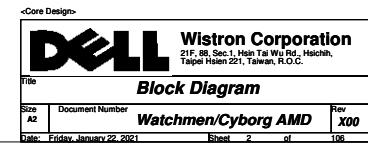
Rev

**X00**

Date: Friday, January 22, 2021

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D

C

B

A

(Blanking)

<Core Design>

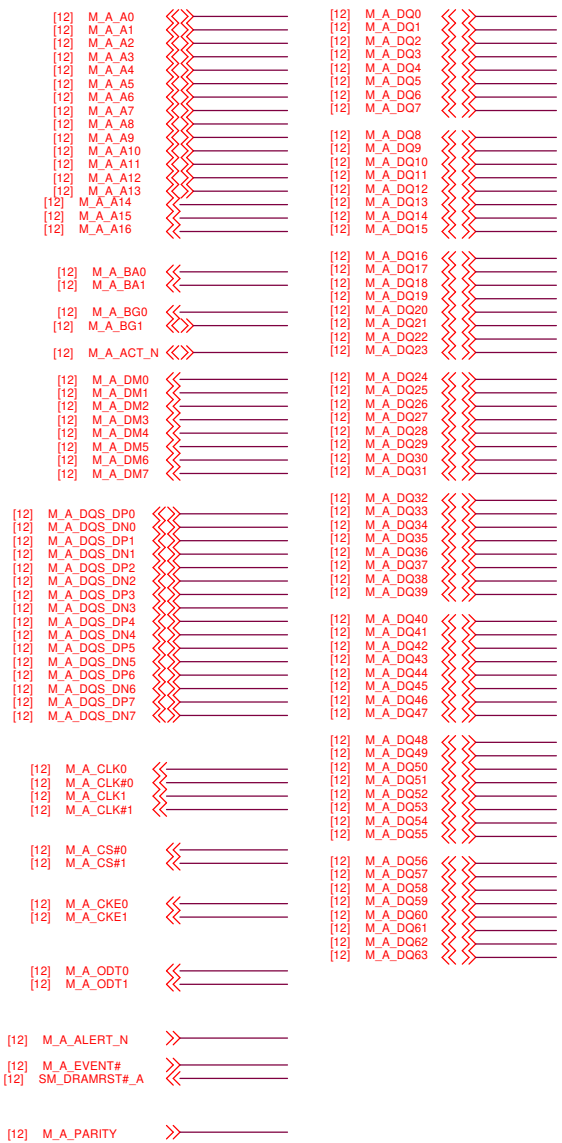


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Title				
CPU (RSVD)				
Size	Document Number			Rev
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SSID = CPU

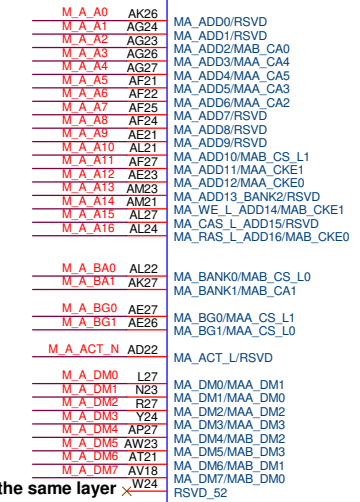


APU Type 2 does not support Channel A

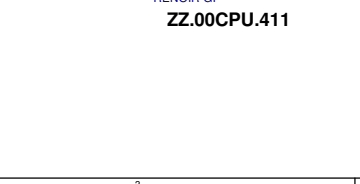
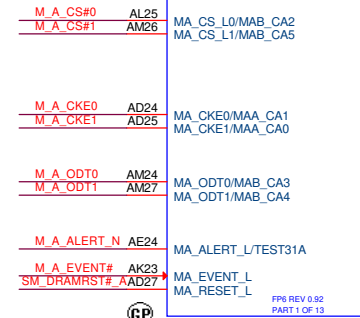
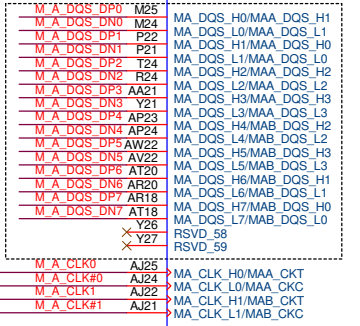
ADD, CMD, CTL, 40Ω  
DATA CHECK, 50Ω  
Misc. 40~60Ω  
DDR CLK, 72Ω  
DQS, 80Ω

DDR4  
Channel A to SO-DIMM

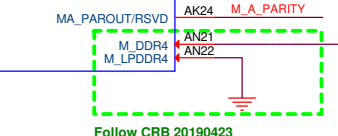
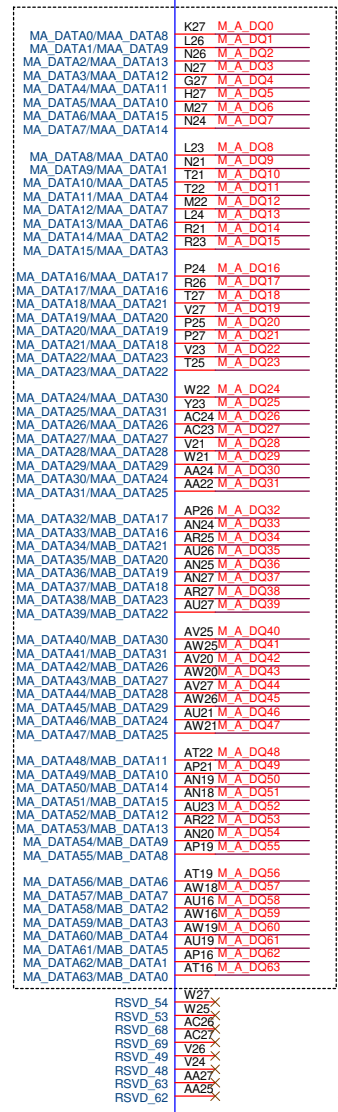
ADD and CLK on the sam layer



DM, DQ & DQS on the same layer



DM, DQ & DQS on the same layer



Follow CRB 20190423

1D2V\_S3

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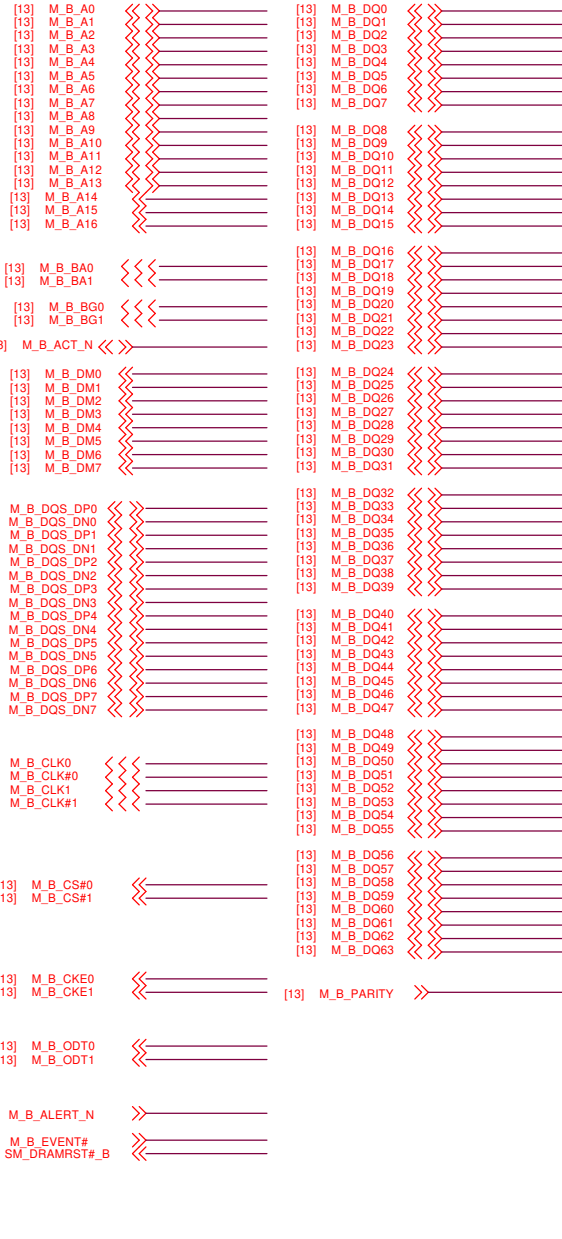
Title: **CPU (DDR4 CHA)**

Size A3 Document Number: **Watchmen/Cyborg AMD** Rev: **X00**

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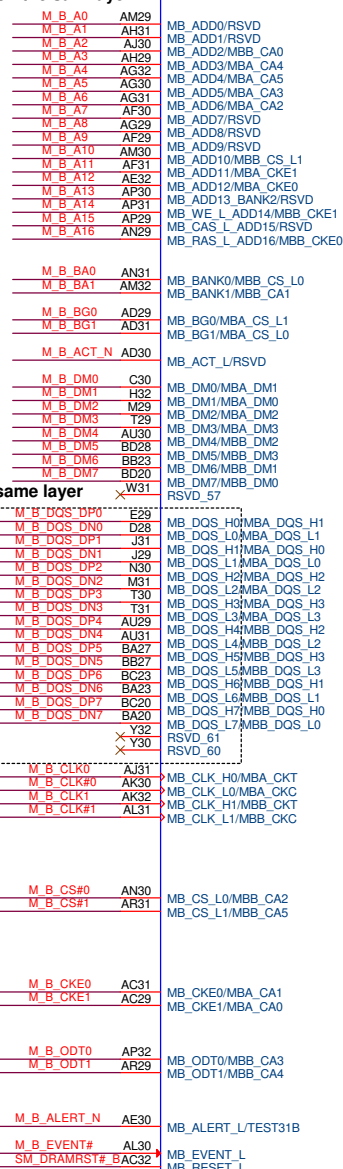


## SSID = CPU

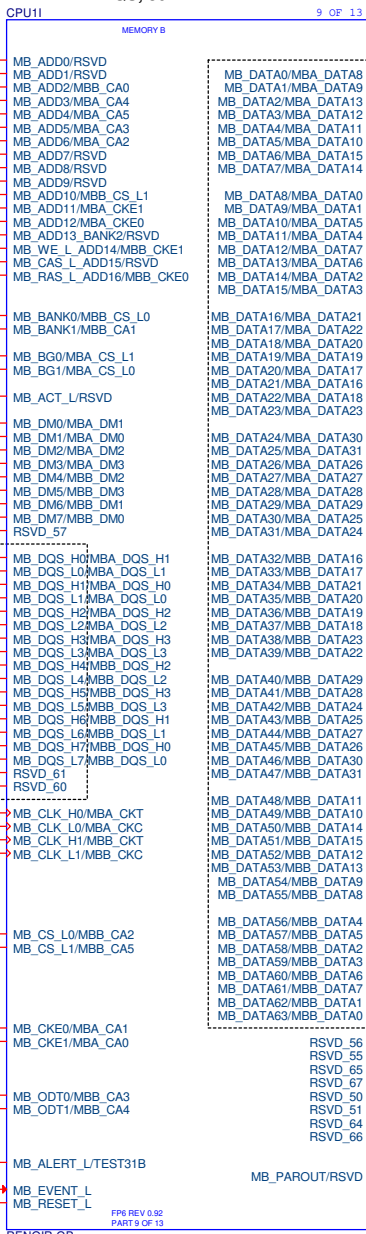


## DDR4 Channel B to SO-DIMM

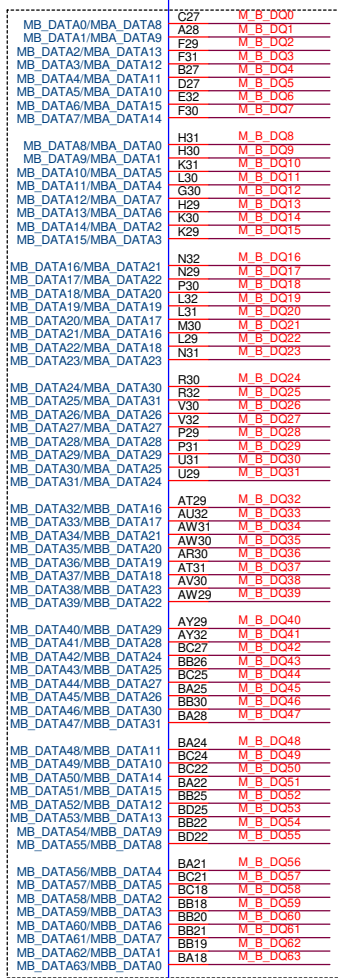
### ADD and CLK on the sam layer



ADD, CMD, CTL, 40Ω  
DATA CHECK, 50Ω  
Misc. 40~60Ω  
DDR CLK, 72Ω  
DQS, 80Ω



### DM, DQ & DQS on the same layer



Signal GRP	Signal			
Clocks	CLK			
Address	ADD	BANK	BG	
Command	RAS_L	CAS_L	WE_L	ACT
Control	CKE	ODT	CS_L	
Data	Data	DM	DQS	
Misc.	M_RESET_L	M_EVENT_L	M_ALERT	



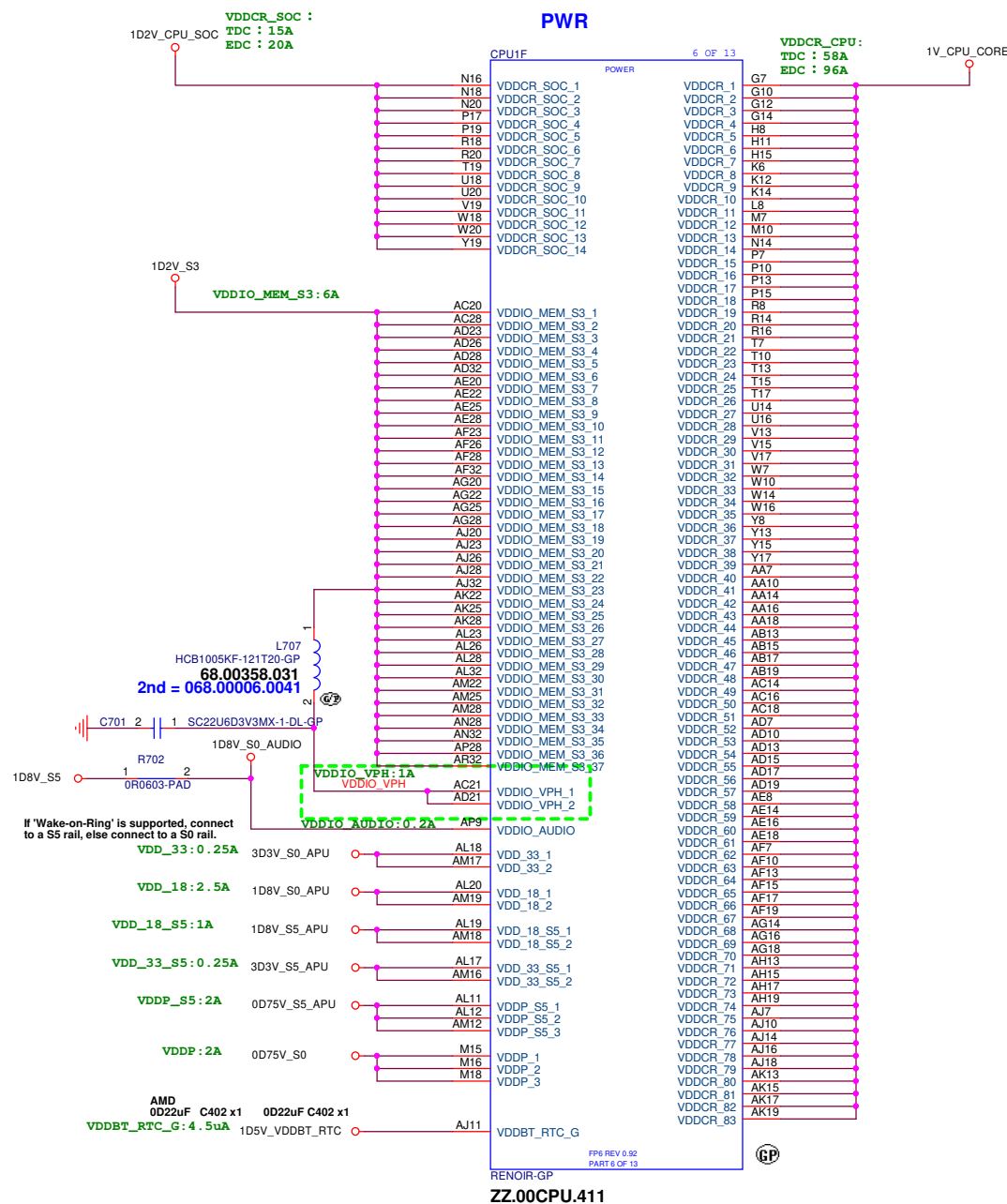
**Table 7. FP6 Processor Voltage Supply Currents for AMD Family 17h Models 60h-6Fh Processors**

**NOTICE:** To identify the proper requirements for AMD Family 17h Models 60h and AMD Family 17 Models 68h, see notes 8 and 9.

Supply <sup>1</sup>	Nominal Voltage at Pkg Ball (V) <sup>2</sup>	Condition	SYSTEM CONFIGURATION					
			1 10 W	2 15 W	3 25 W	4 35 W	5 45 W	6 54 W
VDDCR_VDD	Variable	TDC <sup>3</sup>	20	33	44	51	58	
	(0.6-1.55) <sup>5</sup>	EDC	34	50 <sup>8</sup> /70 <sup>9</sup>	70	90	96	
		Max Loadstep <sup>4</sup>	29	43 <sup>8</sup> /65 <sup>9</sup>	65	76	84	
VDDCR_SOC	Variable	TDC <sup>3</sup>	10	13	15			
	(0.6-1.55) <sup>5</sup>	EDC	13	17	20			
		Max Loadstep <sup>4</sup>	10	13	15			
VDDIO_MEM_S3 <sup>6</sup>	1.10	TDC	6.00					
	1.20	TDC	6.00					
VDDIO_VPH <sup>7</sup>	1.20	TDC	1.00					
	1.80	TDC	1.00					
VDDP	0.75	TDC	2.00					
VDDP_S5	0.75	TDC	2.00					
VDD_18	1.80	TDC	2.50					
VDD_18_S5	1.80	TDC	1.00					
VDD_33	3.30	TDC	0.25					
VDD_33_S5	3.30	TDC	0.25					
VDDIO_AUDIO	1.20	TDC	0.20					
	1.50	TDC	0.20					
	1.80	TDC	0.20					
VDDBT_RTC_G	3.00	TDC	4.5 $\mu$ A					

**Notes:**

1. These specifications are for the processor only. For voltage supplies that are used by other components on the platform, consult documentation for that component to ensure that both specifications are met.
2. A voltage supply must be capable of providing any specified nominal voltage based on processor configuration. An OPN may only support a subset of nominal voltages. Lower nominal voltages may limit performance relative to higher nominal voltages.
3. Current may exceed TDC for variable, limited periods of time, however the average current over any ~100 ms moving time period will be held to less than or equal to the TDC limit.



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Title

**CPU (ALL POWER)**

Size

Document Number

## Watchmen/Cyborg AMD

Rev

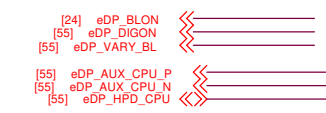
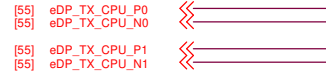
Date: Friday, January 22, 2021

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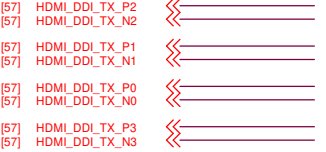


SSID = PCH

eDP



HDMI



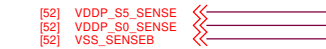
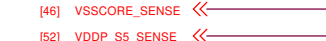
TYPE-C DP



HDT

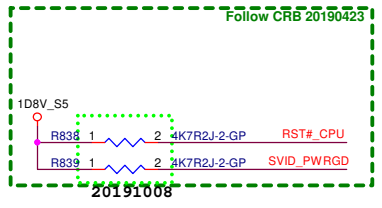


SVID

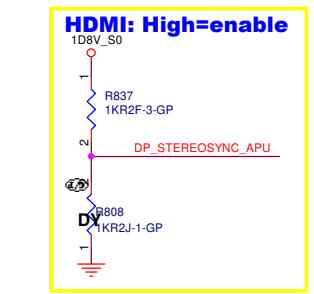
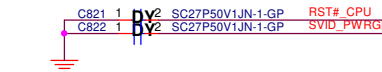
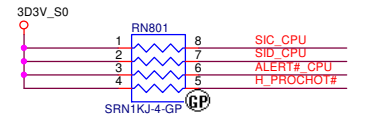


DISPLAY/SVI/JTAG/TEST

APU Type I(CZ): 1D8V  
APU Type II(CZ-L): 3D3V

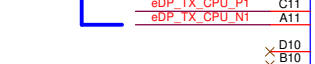


HDT&HDT+:NEED TO POP ON EV/EVT stage

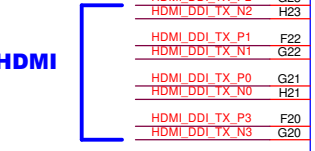


DisplayPort	Device
0	eDP
1	HDMI out

eDP

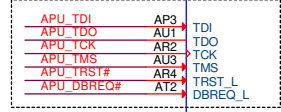


HDMI

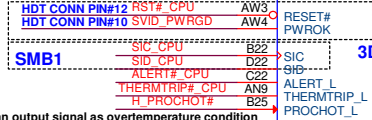


SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

HDT

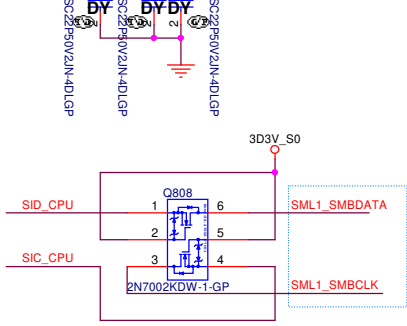
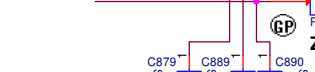


HDT

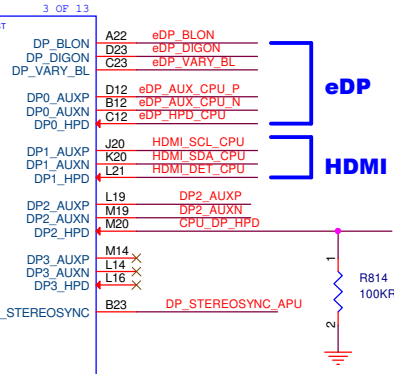
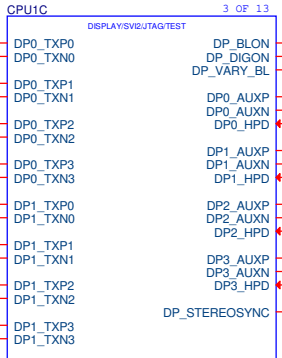


an output signal as overtemperature condition

SVID



75.27002.F7C  
2nd = 075.67002.007C  
3rd = 075.063D1.007C  
4th = 075.07002.0A7C

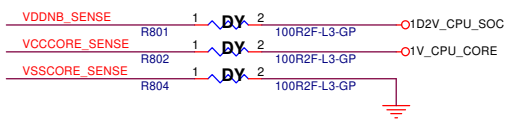
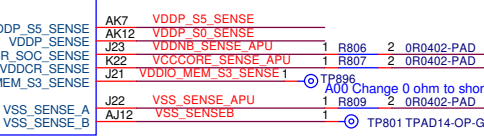
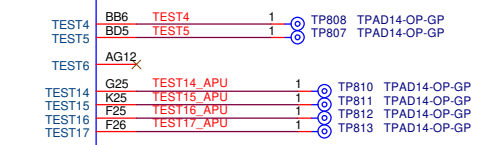


APU Type I 1D8V  
APU Type II 3D3V

PINOUT	Description
DP_BLON	BL_ENABLE
DP_DIGON	LCD_VCC_ENABLE
DP_VARY_BL	BL_PWM

DisplayPort	Device
0	eDP
1	HDMI
2	
3	DP

TYPE-C DP



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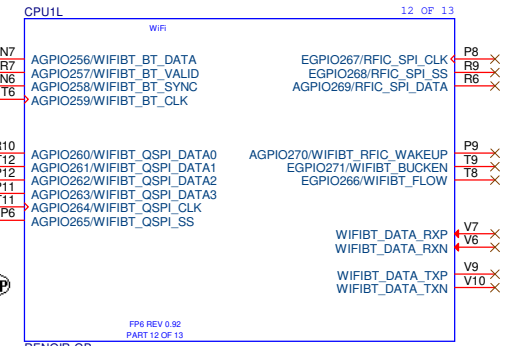
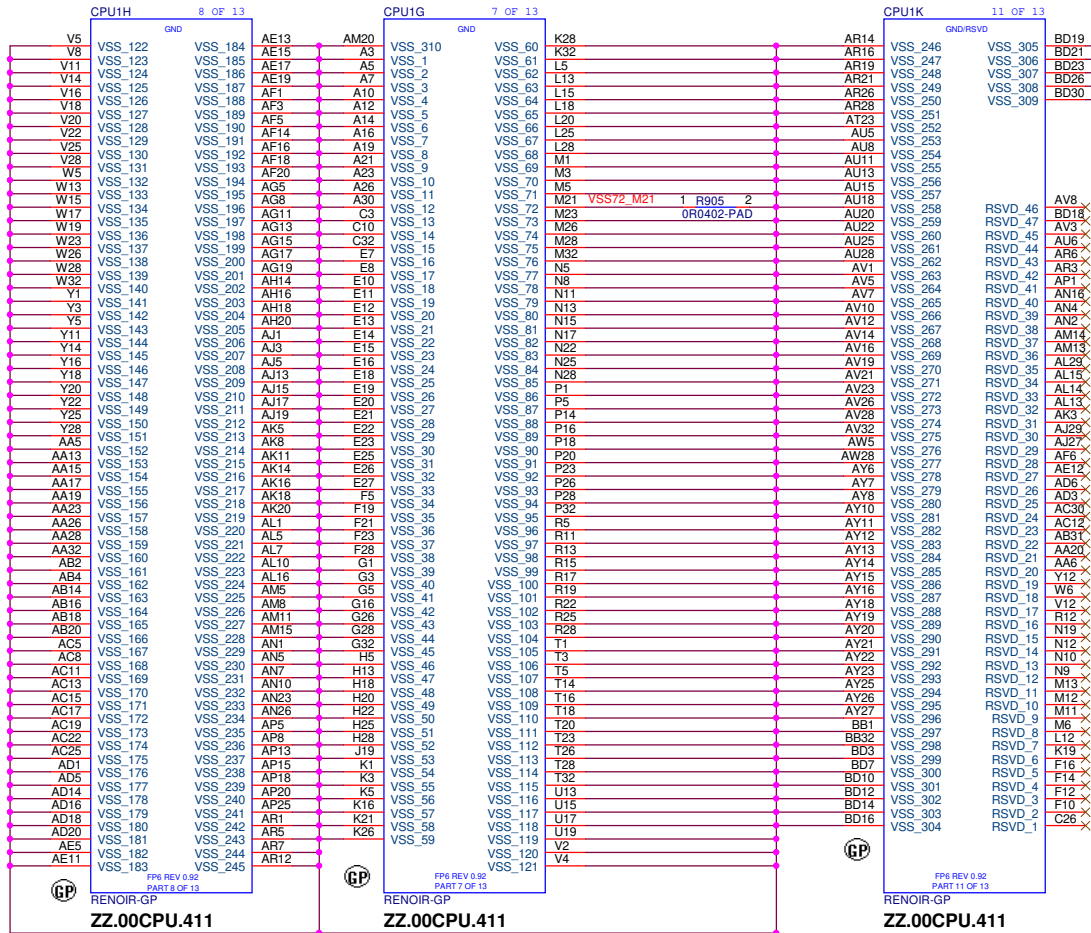
Title: **CPU (DP/SVID/HDT/TEST)**

Size: A3 Document Number: **Watchmen/Cyborg AMD** Rev: **X00**

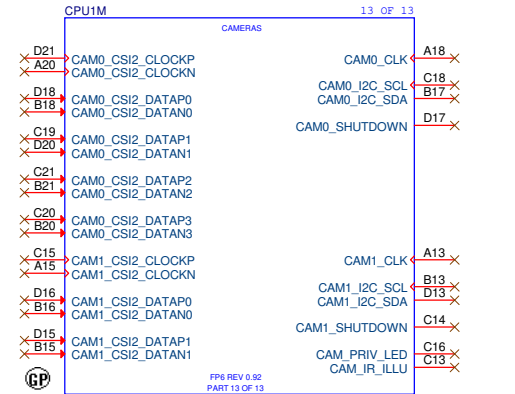
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## VSS

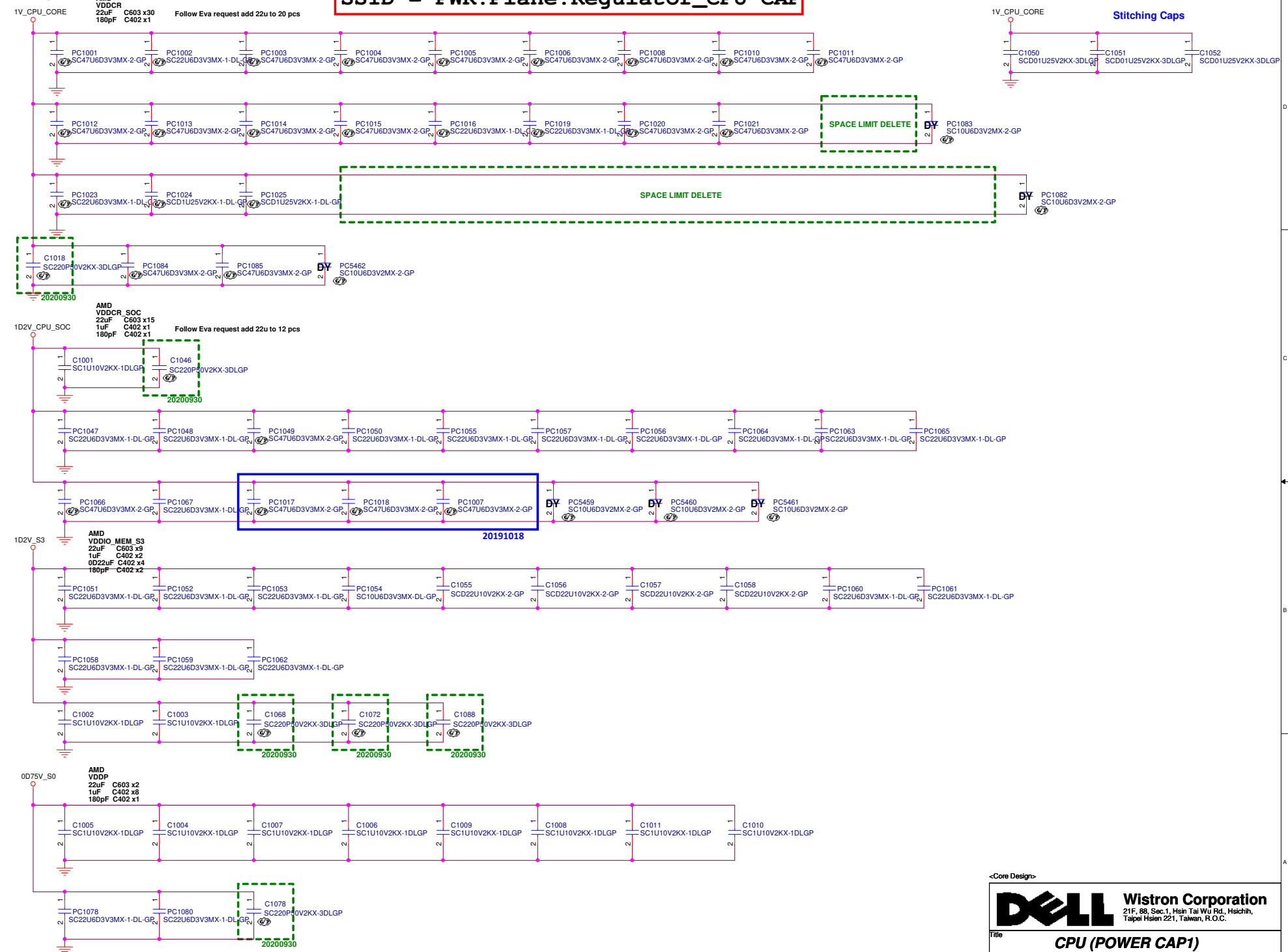


RENOIR-GP  
ZZ.00CPU.411





APU Caps



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Title: **CPU (POWER CAP1)**

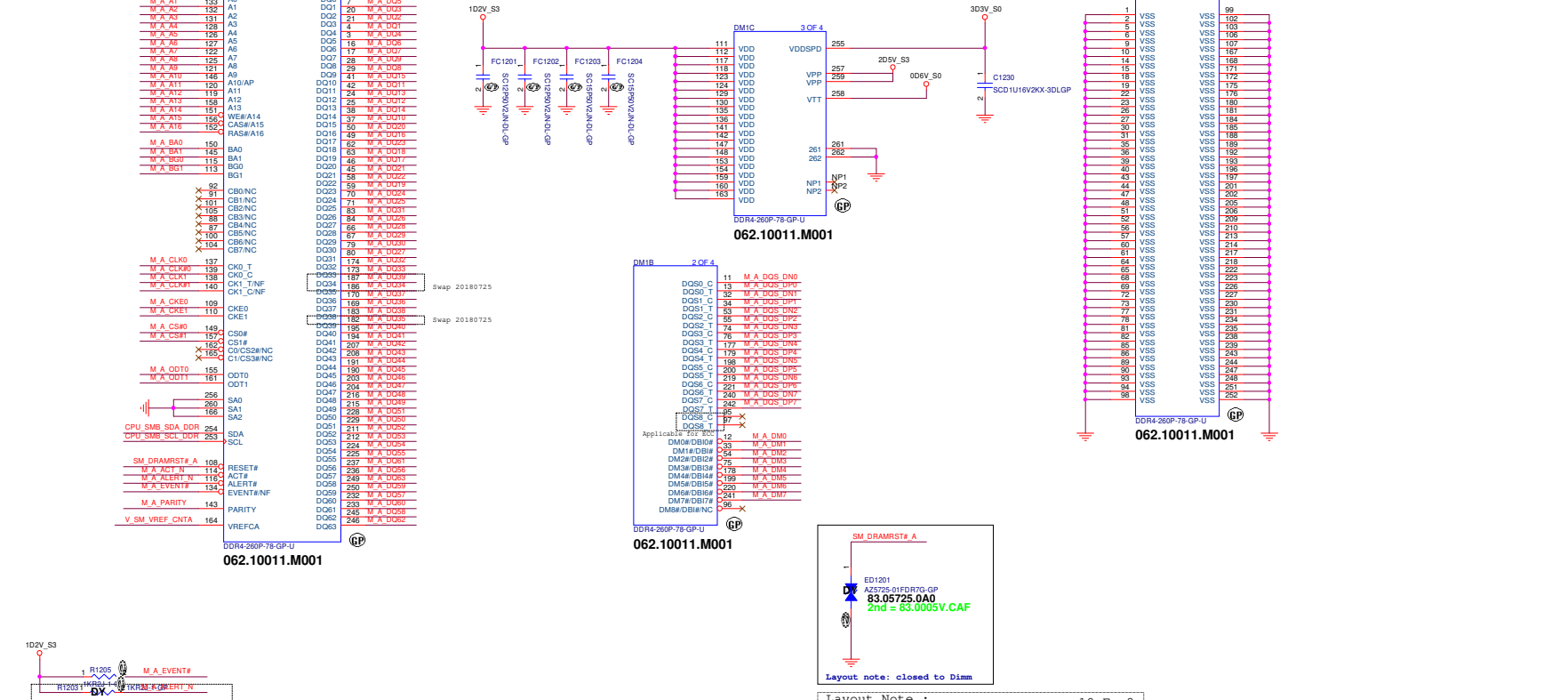
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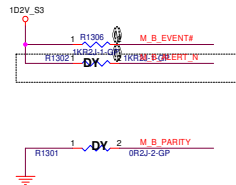
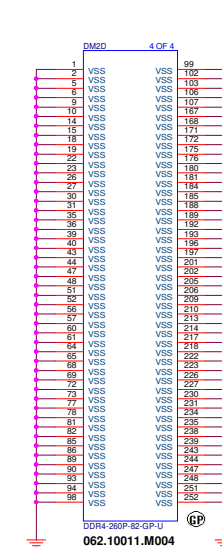
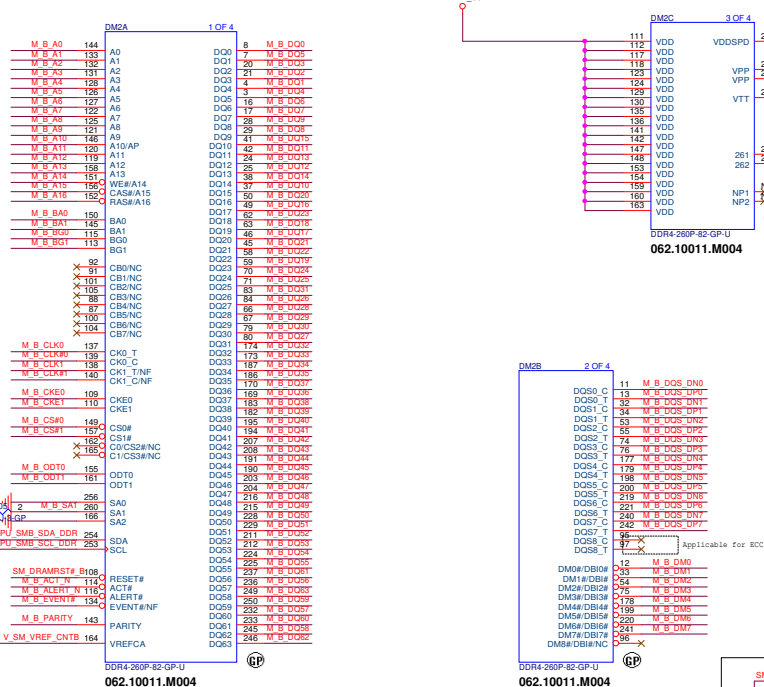
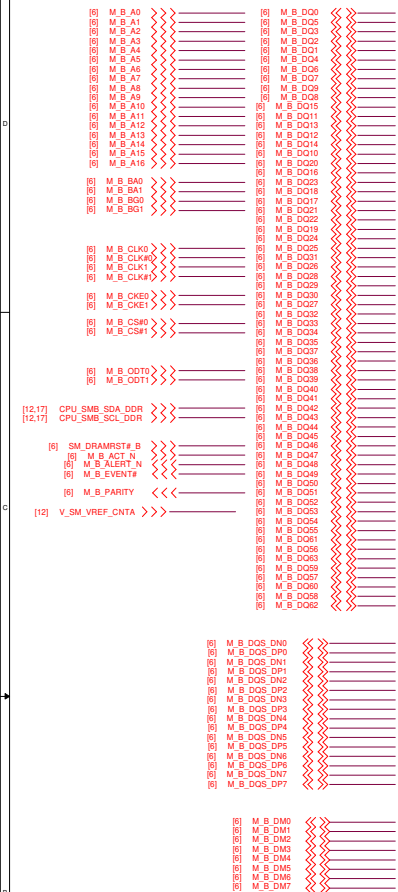


Phylogenetic tree showing relationships between DM1A and DM1D. DM1A is 1 of 4, and DM1D is 4 of 4. The tree shows a split between DM1A and DM1D, with DM1A having a bootstrap value of 144 and DM1D having a bootstrap value of 8.

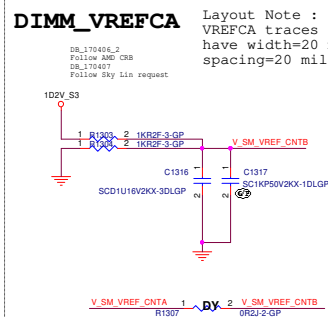




## Standard Type

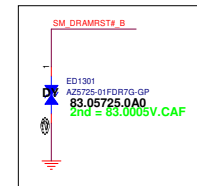


Layout note: closed to Dimm

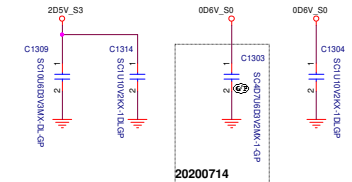
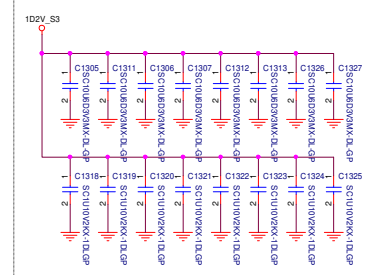


## SPD Address of DIMMB

SPD SA2	0
SPD SA1	1
SPD SA0	0



Layout Note :	10uF x8
Place these Caps near DIMM2	1uF x8



&amp;ltCore Design&gt;



DDR (DDR4-SODIMM2\_CHB)

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D

D

C

C

B


B

A

A

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<Core Design>

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Title <b>DDR (RSVD)</b>					
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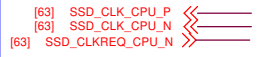
(Blanking)

<Core Design>

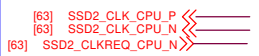
			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>DDR (RSVD)</b>					
Size A4	Document Number <b>Watchmen/Cyborg AMD</b>				Rev <b>X00</b>
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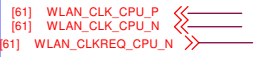
SSD



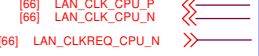
SSD2



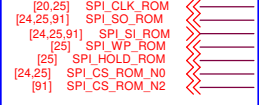
WLAN



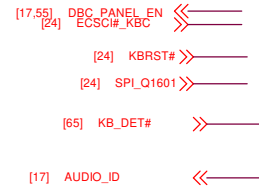
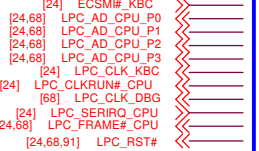
LAN



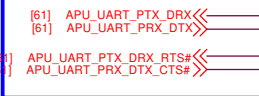
SPI



LPC

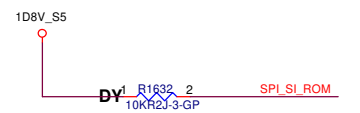
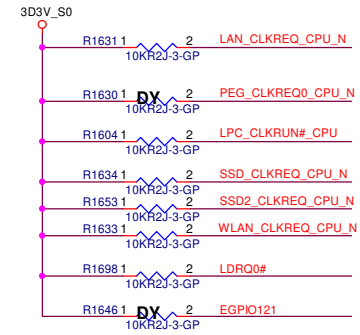


HC WLAN

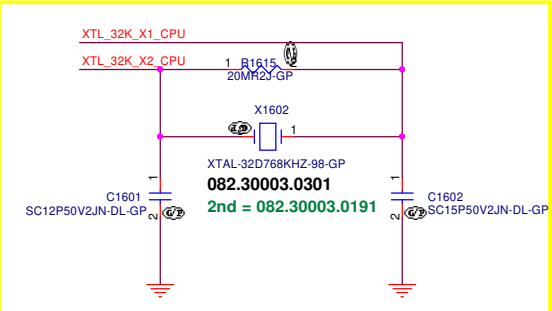
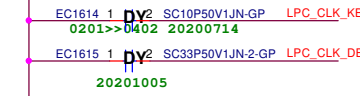
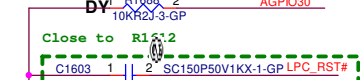


CLK/SATA/USB/SPI/LPC

P	GPP CLK port	Device
0		SSD
1		WLAN
2		NC
3		GPU
4		LAN
5		SSD2
6		NC



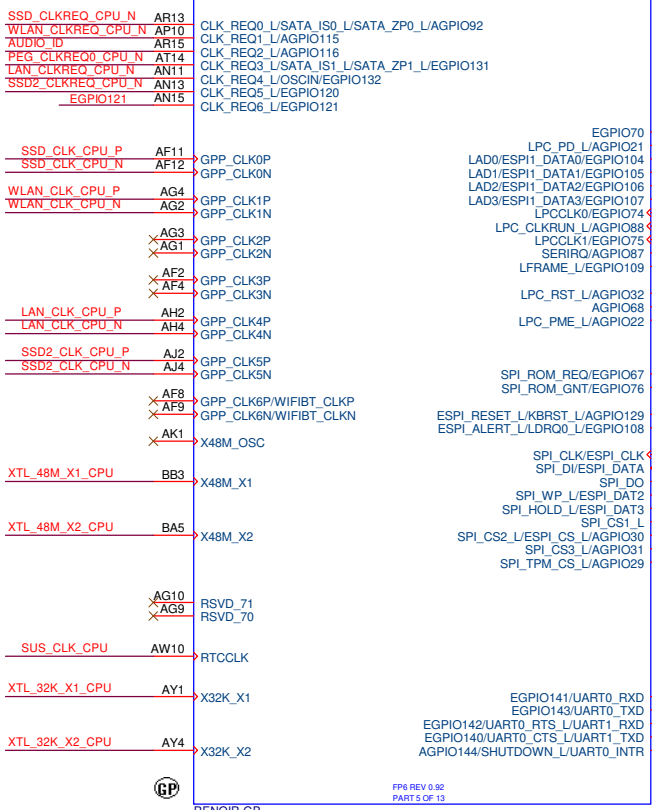
Remove R1635 R1636 for layout space



LPCCLK1/EGPIO75  
CLK\_REQ5\_L  
If unused,  
enable internal pull up or pull down by software.

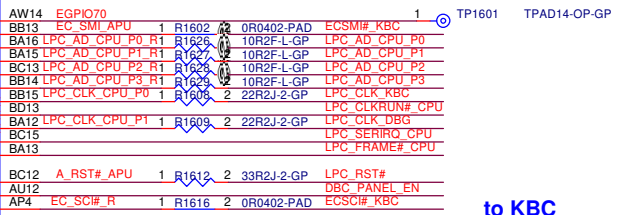
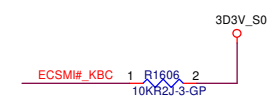
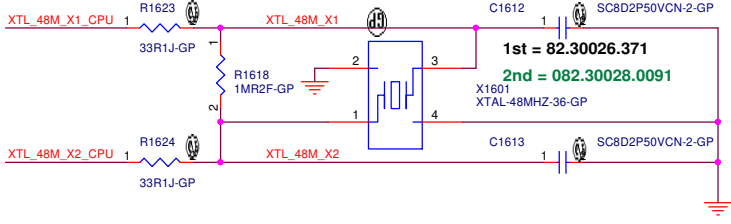
SSD  
WLAN

LAN  
SSD2



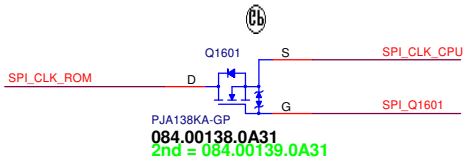
ZZ.00CPU.411

Note:  
C1612 and C1613 values determine CL value of the oscillation circuit.  
If Negative Resistance is too low, that may cause crystal resonator stop oscillation or not easy to oscillate.  
If Drive Level is too high, that may cause crystal resonator abnormal oscillation or damaged the main body of quartz.



to KBC

DB. 170410  
Follow BIOS request for AMD  
LPC interface debug



<Core Design>

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

**CPU (CLK/LPC/SPI/UART)**

Size A3	Document Number	Rev X00
<b>Watchmen/Cyborg AMD</b>		
Date: Friday, January 22, 2021	Sheet 16	of 106



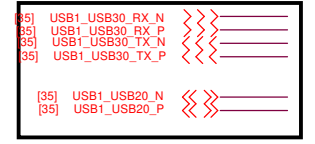
---





Main Func = USB

USB3.0 Port1



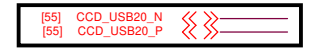
USB3.0 Port2



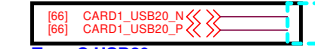
Finger Printer



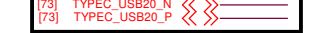
IR Camera



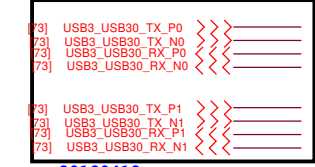
Card Reader



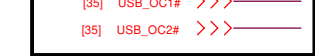
Type C USB20



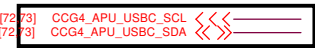
DP Type-C



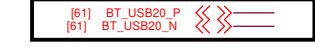
20180418



BT



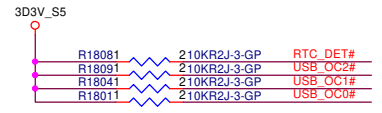
BT



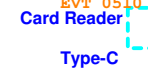
BT



USB_OC#	Type C
USB_OC0#	USB3.0 Power
USB_OC1#	USB3.0 Power
USB_OC2#	USB3.0 Power
USB_OC3#	USB3.0 Power



USB3.0 Port1



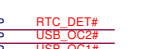
IR Camera



BlueTooth



USB3.0 Port2



BlueTooth



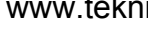
BlueTooth



BlueTooth



BlueTooth



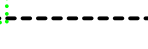
BlueTooth



BlueTooth



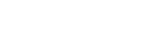
BlueTooth



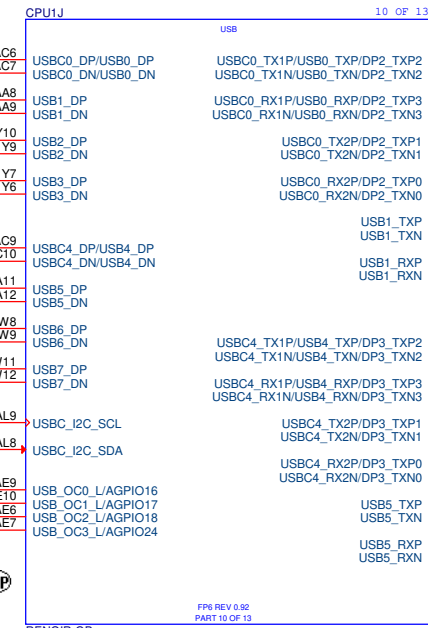
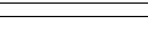
BlueTooth



BlueTooth



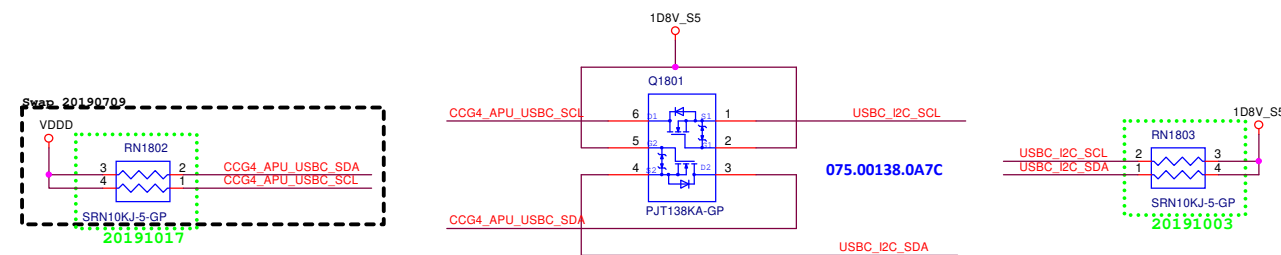
BlueTooth



REN0IR-GP  
ZZ.00CPU.411

AGPIO13/USB\_OC5\_L  
If unused,  
enable internal pull up or pull down by software.

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<Core Design>

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Title: **CPU (USB)**


Size: A3 Document Number: **Watchmen/Cyborg AMD** Rev: **X00**

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<Core Design>



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU (RSVD)**

Size  
A3

Document Number

Date: Friday, January 22, 2021

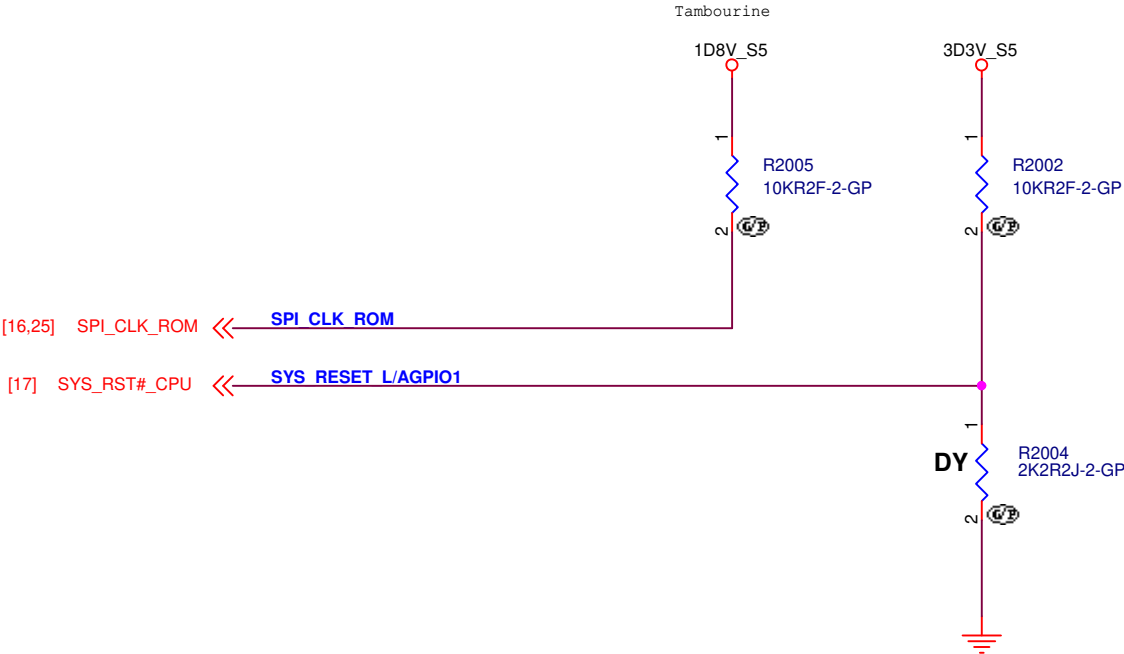
**Watchmen/Cyborg AMD**

Rev  
**X00**

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STRAP PINS



	PIN SPI_CLK NET SPI_CLK_ROM	PIN SYS_RESET_L//AGPIO1 NET SYS_RST#_CPU
PULL HIGH	Configured for internal clock-generator 10kΩ(± 5%) pull-up resistor to VDD_18 (DEFAULT)	Normal powerup / reset timing 10kΩ(± 5%) pull-up resistor to VDD_33_S5 (DEFAULT)
PULL LOW	Reserved	Reserved

<Core Design>

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Title

**CPU (Strap)**

Size  
A4

Document Number

Rev  
**X00**

Date: Friday, January 22, 2021


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Title

CPU (RSVD)

Size  
A3

Document Number

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X00

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Title

**CPU (RSVD)**

Size  
A3

Document Number

Date: Friday, January 22, 2021

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X00

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (RSVD)

Size  
A3

Document Number

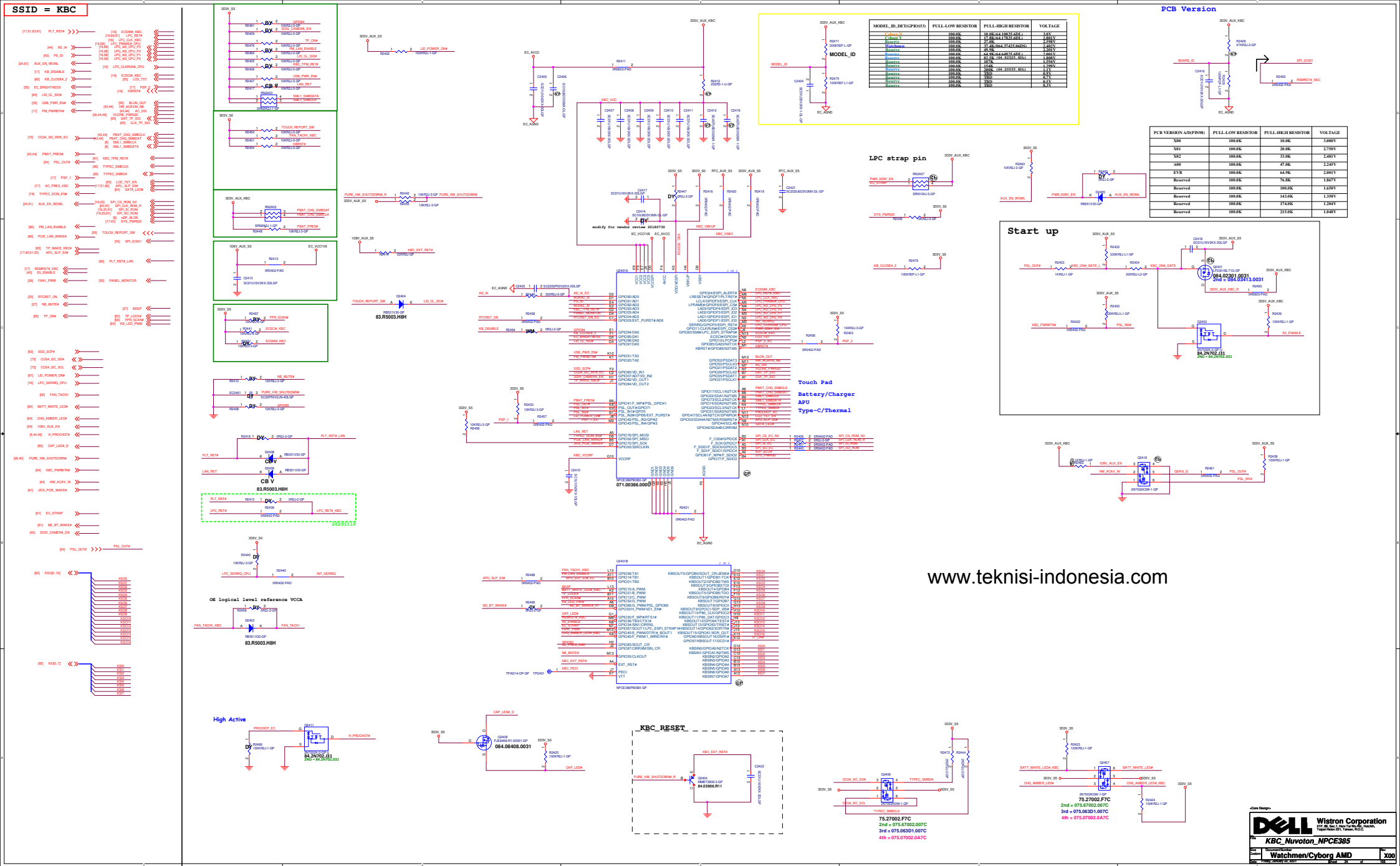
Date: Friday, January 22, 2021

**Watchmen/Cyborg AMD**

Rev  
X00

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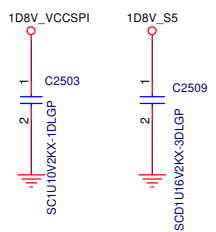
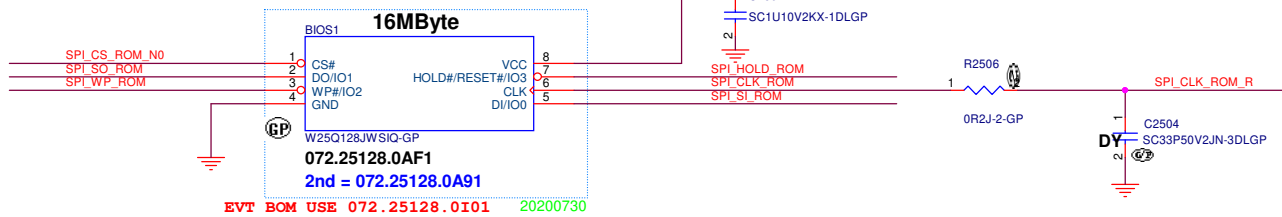


# SSID = Flash.ROM

1D8V\_VCCSPI

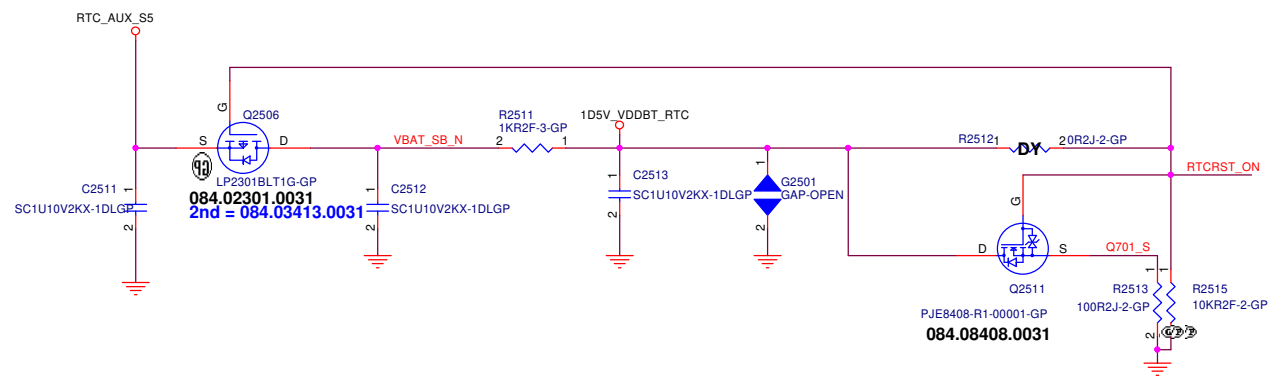
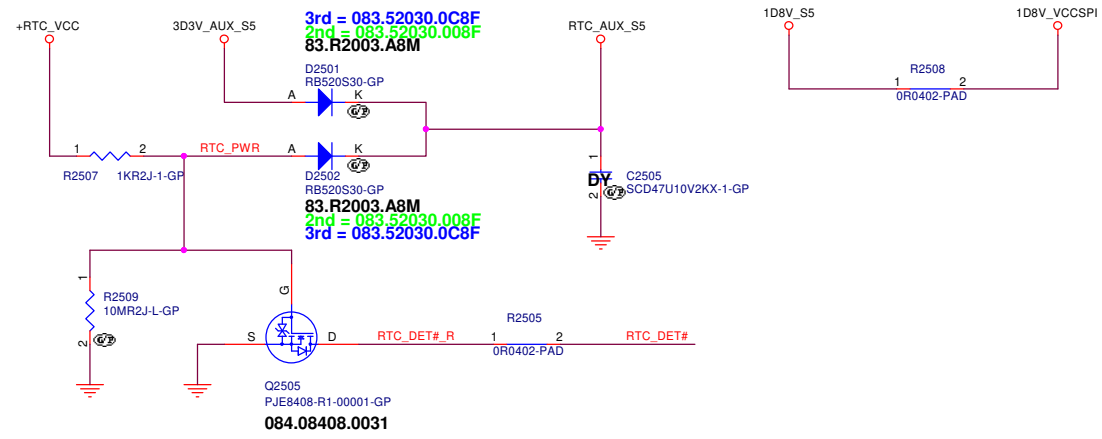
R25011 210KR2J-3-GP SPI\_SO\_ROM  
R25021 210KR2J-3-GP SPI\_CS\_ROM\_N0  
R25031 210KR2J-3-GP SPI\_WP\_ROM  
R25041 210KR2J-3-GP SPI\_HOLD\_ROM

[16,24] SPI\_CS\_ROM\_N0 >>>  
[16,24,91] SPI\_SO\_ROM >>>  
[16] SPI\_WP\_ROM >>>  
  
[16] SPI\_HOLD\_ROM <<<  
[16,24,91] SPI\_SI\_ROM <<<  
[24,91] SPI\_CLK\_ROM\_R <<<  
[16,20] SPI\_CLK\_ROM <<<



# SSID = RBAT

[24] RTCRST\_ON >>>  
[18] RTC\_DET# >>>










[29,66] AUD\_SLEEVE <<< \_\_\_\_\_  
[29,66] AUD\_RING <<< \_\_\_\_\_

NEED TO BE PLACE NEAR PCH 20190813



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<Core Design>

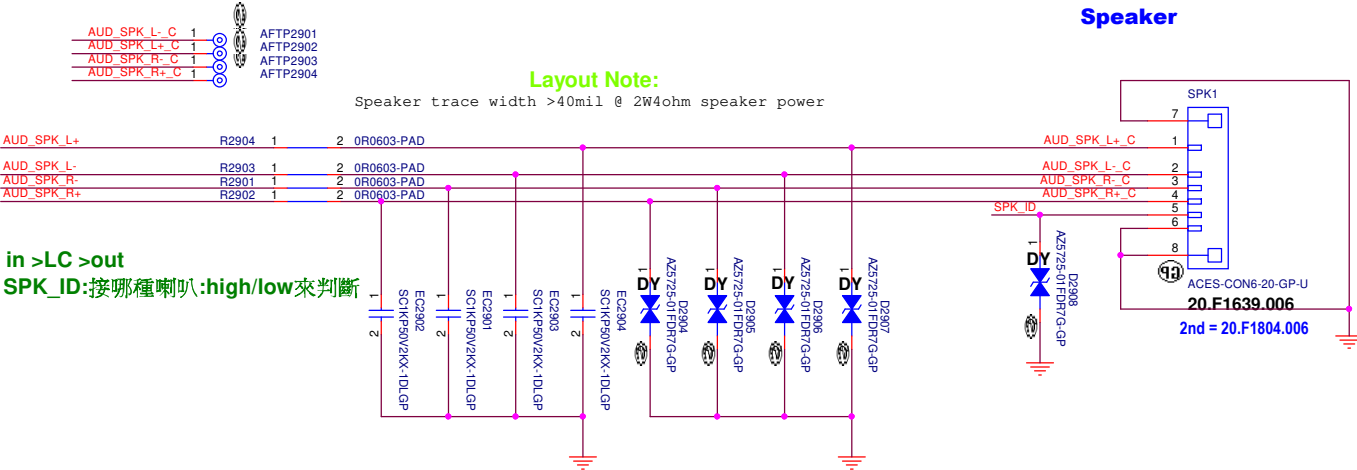
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Audio</b>			
Size A4	Document Number		Rev
	<b>Watchmen/Cyborg AMD</b>		<b>X00</b>
Date: Friday, January 22, 2021		Sheet 28 of	106



Main Func = Audio

[27] AUD\_SPK\_R+ >>>  
[27] AUD\_SPK\_R- >>>  
[27] AUD\_SPK\_L+ >>>  
[27] AUD\_SPK\_L- >>>

[17] SPK\_ID <<<



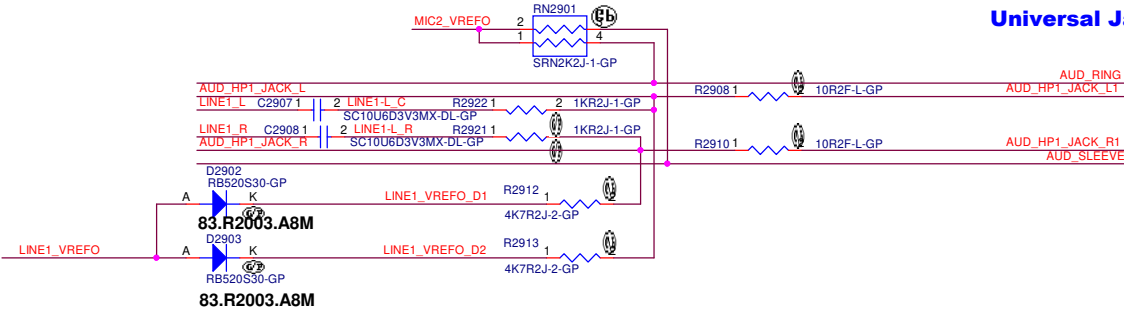
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L-
Pin4	SPK_L+

From Codec

[27] MIC2\_VREFO >>>  
[27,29,66] AUD\_RING <<<  
[27] AUD\_HP1\_JACK\_L >>>  
[27] LINE1\_L >>>  
[27] LINE1\_R >>>  
[27] AUD\_HP1\_JACK\_R >>>  
[27,29,66] AUD\_SLEEVE <<<  
[27] LINE1\_VREFO >>>

To IO Board

[27,29,66] AUD\_RING <<<  
[66] AUD\_HP1\_JACK\_L1 <<<  
[66] AUD\_HP1\_JACK\_R1 <<<  
[27,29,66] AUD\_SLEEVE <<<






Main Func = Audio

(Blanking)

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)</b>		
Size A4	Document Number <b>Watchmen/Cyborg AMD</b>	Rev <b>X00</b>
Date: Friday, January 22, 2021		Sheet 30 of 106




Main Func = LAN

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Title

**LAN (Reserved)**

Size	Document Number	Rev
A3	<b>Watchmen/Cyborg AMD</b>	<b>X00</b>


Date: Friday, January 22, 2021	Sheet 31 of 106
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Main Func = LAN

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**XFOM&RJ45 (Reserved)**

Size

A3

Document Number

**Watchmen/Cyborg AMD**

Rev

**X00**

Date: Friday, January 22, 2021

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Main Func = USB2.0

<Core Design>

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Title					
<b>USB Charger</b>					
Size	Document Number				Rev
A4	<b>Watchmen/Cyborg AMD</b>				<b>X00</b>
Date: Friday, January 22, 2021			Sheet 34 of 106		








Main Func = USB Charger

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

***USB Charger***

Size  
A4

Document Number  
***Watchmen/Cyborg AMD***

Rev  
***X00***


Date: Friday, January 22, 2021

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<Core Design>



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Title

Size

A3

Document Number

**Watchmen/Cyborg AMD**

Date: Friday, January 22, 2021

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Rev


**X00**

**Reserved**



Main Func = USB HUB

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB HUB</b>			
Size	Document Number		Rev
A4	<b>Watchmen/Cyborg AMD</b>		<b>X00</b>
Date: Friday, January 22, 2021		Sheet 38 of	106



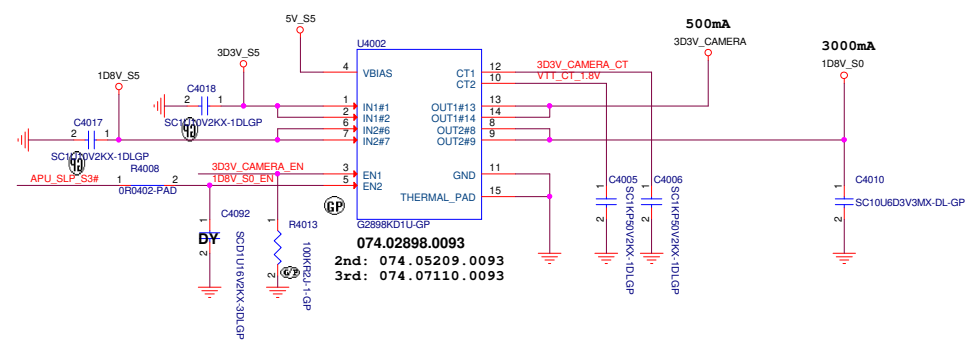
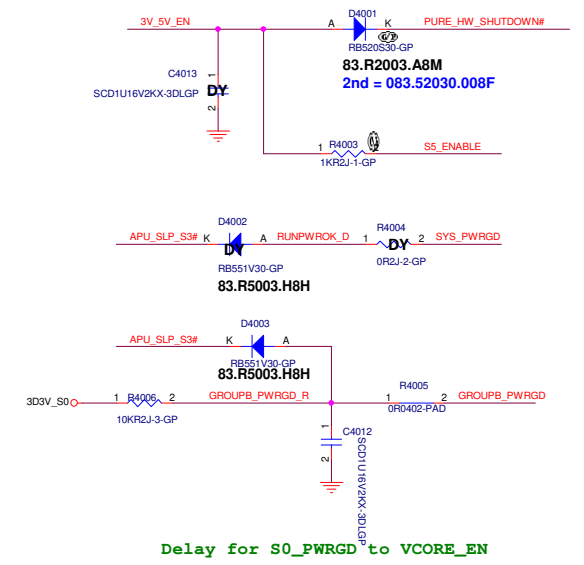
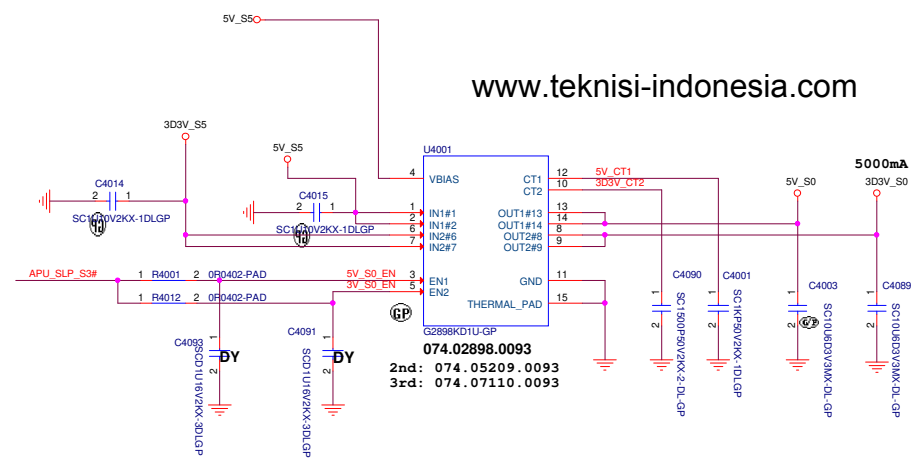




# Power Sequence

- [17,24,51,52] APU\_SLP\_S3# >>
- [45] 3V\_5V\_EN <<
- [24,26] PURE\_HW\_SHUTDOWN# >>
- [24] S5\_ENABLE >>
- [17,24] SYS\_PWRGD >>
- [44,46] GROUPB\_PWRGD <<
- [24] 3D3V\_CAMERA\_EN >>

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<Core Design>

**DELL** Wistron Corporation  
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Title <b>Power Plane Enable&amp;Sequence</b>		
Size Custom	Document Number <b>Watchmen/Cyborg AMD</b>	Rev <b>X00</b>
Date: Friday, January 22, 2021	Sheet 40	of 106



Main Func = Power Plane & Sequence

(Blanking)

<Core Design>



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Title

***Connected\_Standby(1/2)+DS3***

Size  
A4

Document Number

***Watchmen/Cyborg AMD***

Rev  
***X00***


Date: Friday, January 22, 2021

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<Core Design>



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Title

Connected\_Standby(2/2)

Size

A3

Document Number

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Date: Friday, January 22, 2021

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106



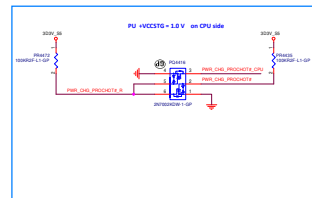




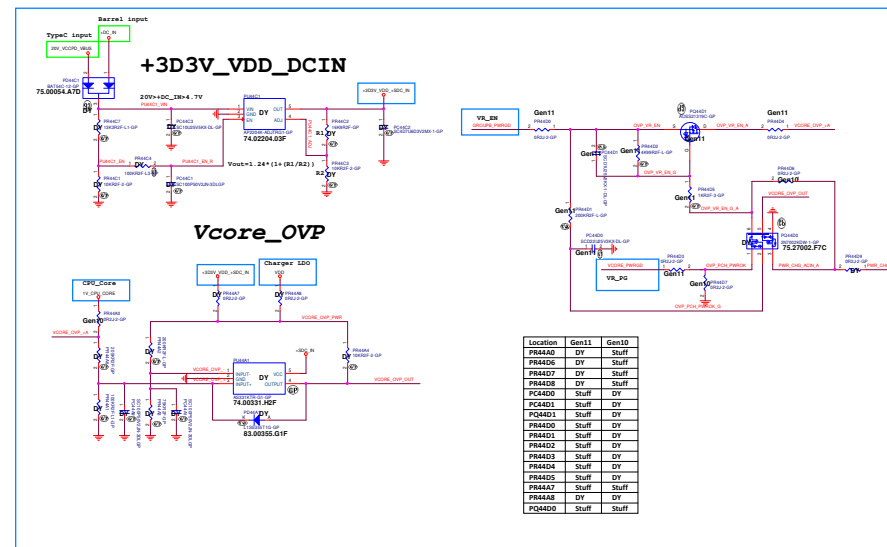
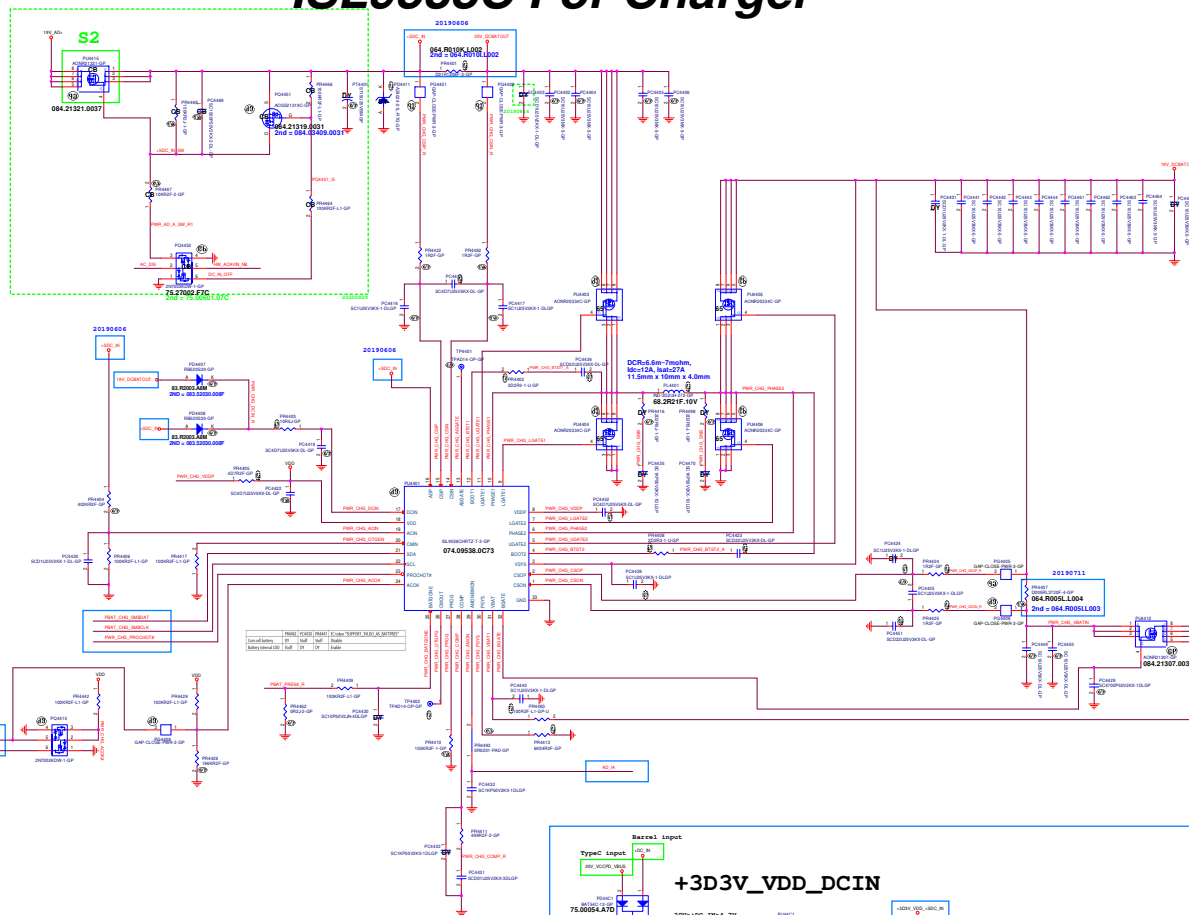
[illegible]

The diagram illustrates the Prochot architecture, showing three parallel processing paths. Each path starts with a 'Prochot' block, followed by a 'Read (R00001) (FAD-GP)' block, and then a 'PWR\_CHG\_PROCHOTx\_CPU' block. The paths are labeled 'H Prochot', 'PWR\_CHG\_TIP\_3', 'typeC Prochot', and 'PWR\_CHG\_BP\_3'. The final output is 'Barrel Prochot'.

PROPOSED REQUIREMENTS			DEFINITION OF REQUIREMENTS		DEFINITION OF REQUIREMENTS	
TYP MIN	MAX	EXC	DEFINITION OF REQUIREMENTS	DEFINITION OF REQUIREMENTS	DEFINITION OF REQUIREMENTS	
0	0	1	7330340	No	0.676	
2.47	1.640	No	7330340	No	1.5	
2.47	1.640	No	7330340	No	1.5	
28.0	7330340	Yes	7330340	Yes	0.676	
63.2	7330340	Yes	7330340	Yes	1.5	
63.2	7330340	Yes	7330340	Yes	1.5	
71.9	1.640	No	7330340	No	0.676	
71.9	1.640	No	7330340	No	1.5	
92.8	7330340	Yes	7330340	Yes	1.5	
93.1	7330340	Yes	7330340	Yes	1.5	
138	7330340	No	7330340	No	0.676	
138	7330340	No	7330340	No	0.676	
147	1.640	No	7330340	No	2.5	
147	1.640	No	7330340	No	1.5	
262	7330340	Yes	7330340	Yes	0.676	
262	7330340	Yes	7330340	Yes	1.5	
267	7330340	Yes	7330340	Yes	1.5	
267	7330340	Yes	7330340	Yes	0.676	
275	1.640	No	7330340	No	2.5	
287	7330340	Yes	7330340	Yes	0.676	
287	7330340	Yes	7330340	Yes	1.5	
348	7330340	No	7330340	No	0.676	
348	7330340	No	7330340	No	1.5	



Follow customer circuits.

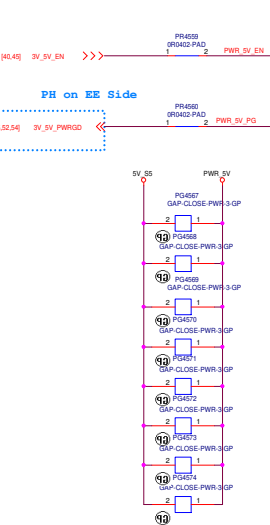


Location	Gen11	Gen12
PR44A0	DY	Stuff
PR44D6	DY	Stuff
PR44D7	DY	Stuff
PR44D8	DY	Stuff
PC44D0	Stuff	DY
PC44D1	Stuff	DY
PQ44D1	Stuff	DY
PR44D0	Stuff	DY
PR44D1	Stuff	DY
PR44D2	Stuff	DY
PR44D3	Stuff	DY
PR44D4	Stuff	DY
PR44D5	Stuff	DY
PR44A7	Stuff	Stuff
PR44A8	DY	DY
PQ44D0	Stuff	Stuff

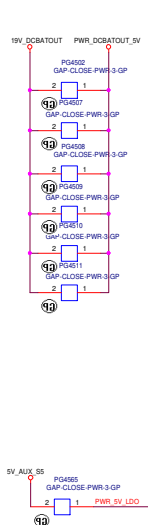


SSID = PWR.Plane.Regulator\_5V

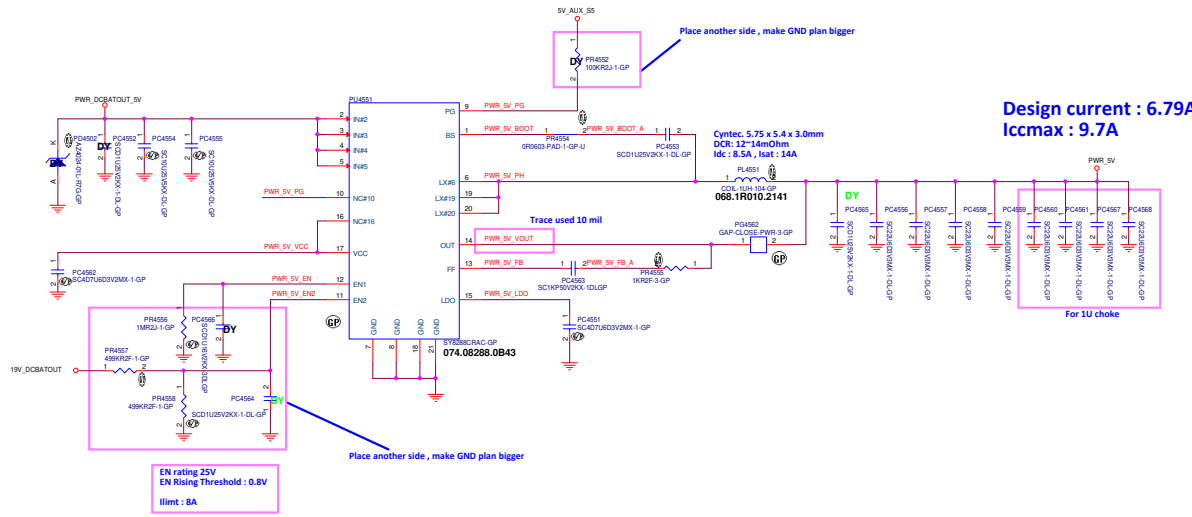
OFFPAGE-Signal



OFFPAGE-GAP

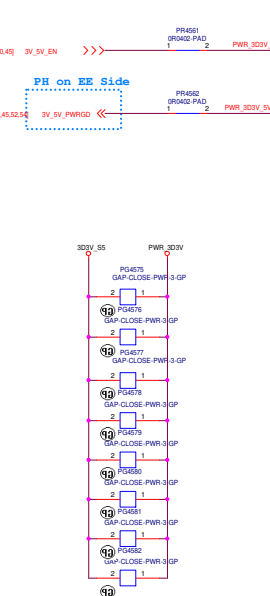


# SY8288C For 5V



SSID = PWR.Plane.Regulator\_3D3V

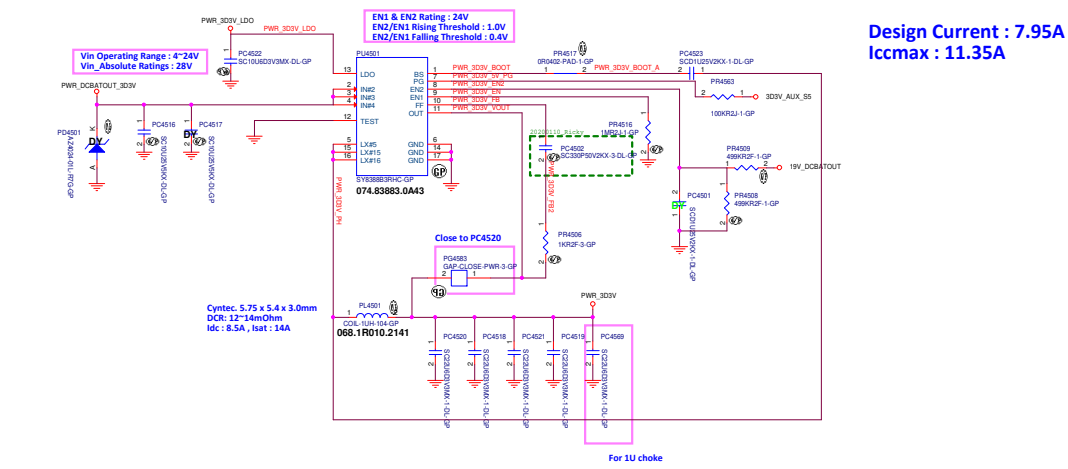
OFFPAGE-Signal



OFFPAGE-GAP



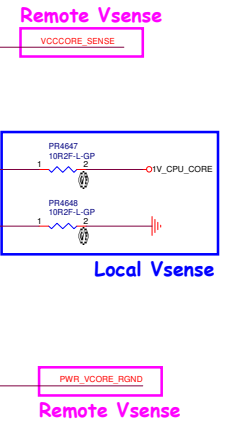
# SY8388B3 For 3D3V



FPR S5 SSO 20191209 REMOVE ALL

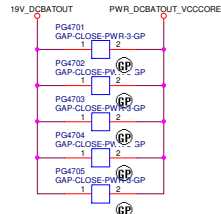


[8,24,44]	H_PROCHOT#	←	
[8]	SVID_ALERT_N_CPU	→	SVID_ALERT_N_CPU
[8]	SVID_CLK_CPU	→	SVID_CLK_CPU
[8]	SVID_DATA_CPU	→	SVID_DATA_CPU
[24,26,44]	VCORE_PWRGD	←	VCORE_PWRGD
[40,44]	GROUPB_PWRGD	→	GROUPB_PWRGD
[8,68]	SVID_PWRGD	←	SVID_PWRGD
[8]	VSSCORE_SENSE	→	VSSCORE_SENSE
[8]	VCCCORE_SENSE	→	VCCCORE_SENSE
[8]	VDDNB_SENSE	→	VDDNB_SENSE

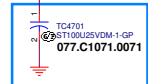




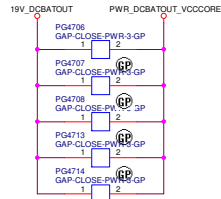
# OFFPAGE



PWR\_DCBATOUT\_VCCOCORE



For acoustic noise



[46] PWR\_VCORE\_LGA >>> PWR\_VCORE\_LGA

[46] PWR\_VCORE\_HGA >>>

[46] PWR\_VCORE\_PHA >>>

[46] PWR\_VCORE\_BOOTA >>>

PR4701 202R3-1-U-GP PWR\_VCORE\_BOOTA\_A

PC4701 SCD1U25V2KX-1-DL-GP

[46.47] PWR\_VCORE\_ISEN1P <<< PWR\_VCORE\_ISEN1P

[46.47] PWR\_VCORE\_ISEN1N <<< PWR\_VCORE\_ISEN1N

[46.47] PWR\_VCORE\_ISEN2P <<< PWR\_VCORE\_ISEN2P

[46] PWR\_VCORE\_LGB >>> PWR\_VCORE\_LGB

[46] PWR\_VCORE\_HGB >>>

[46] PWR\_VCORE\_PHB >>>

[46] PWR\_VCORE\_BOOTB >>>

PR4712 202R3-1-U-GP PWR\_VCORE\_BOOTB\_A

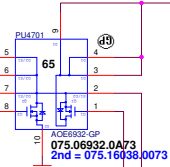
PC4713 SCD1U25V2KX-1-DL-GP

[46.47] PWR\_VCORE\_ISEN2P <<< PWR\_VCORE\_ISEN2P

[46.47] PWR\_VCORE\_ISEN1N <<< PWR\_VCORE\_ISEN1N

PC4710 SCD1U25V2KX-1-DL-GP

[46.47] PWR\_VCORE\_ISEN1P <<< PWR\_VCORE\_ISEN1P



PR4701 202R3-1-U-GP PWR\_VCORE\_BOOTA\_A

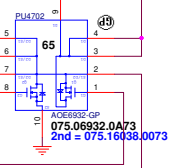
PC4701 SCD1U25V2KX-1-DL-GP



[46.47] PWR\_VCORE\_ISEN1P <<< PWR\_VCORE\_ISEN1P

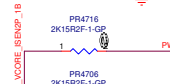
[46.47] PWR\_VCORE\_ISEN1N <<< PWR\_VCORE\_ISEN1N

[46.47] PWR\_VCORE\_ISEN2P <<< PWR\_VCORE\_ISEN2P



PR4712 202R3-1-U-GP PWR\_VCORE\_BOOTB\_A

PC4713 SCD1U25V2KX-1-DL-GP



[46.47] PWR\_VCORE\_ISEN2P <<< PWR\_VCORE\_ISEN2P

[46.47] PWR\_VCORE\_ISEN1N <<< PWR\_VCORE\_ISEN1N

PC4710 SCD1U25V2KX-1-DL-GP

[46.47] PWR\_VCORE\_ISEN1P <<< PWR\_VCORE\_ISEN1P

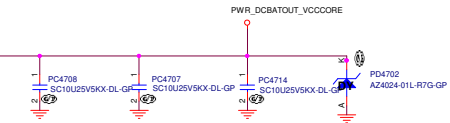
Cyntec: 7.6mm x6.8mmx3.0mm  
DCR: 0.9m Ohm+/-5%  
Idc: 35A, Isat: 41A

PL4701

068.R1510.2191

VCORE : 330uF/6m ohm \* 6pcs+22uF \* 30pcs

TDC=45A  
Imax=70A



PWR\_DCBATOUT\_VCCOCORE

Cyntec: 7.6mm x6.8mmx3.0mm  
DCR: 0.9m Ohm+/-5%  
Idc: 35A, Isat: 41A

PL4702

068.R1510.2191

PR4714 202R3-1-U-GP PWR\_VCORE\_BOOTB\_A

PC4713 SCD1U25V2KX-1-DL-GP

PR4716 2K15R2F-1-GP PWR\_VCORE\_ISEN2P\_2B

PR4706 2K15R2F-1-GP

PC4711 SCD1U25V2KX-1-DL-GP

PR4707 10K92F-2-GP

PC4710 SCD1U25V2KX-1-DL-GP

PR4709 1R2F-GP

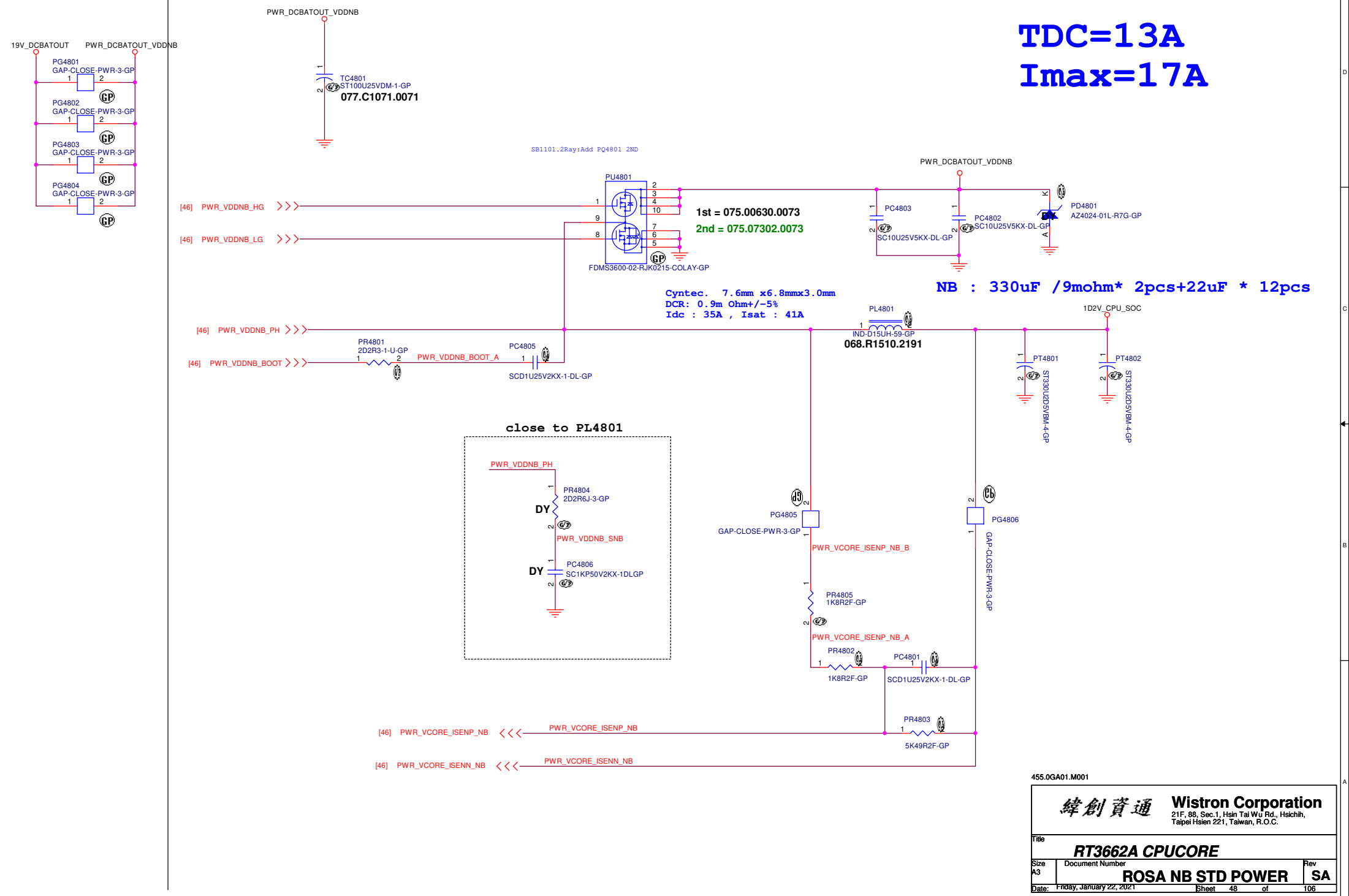
PR4708 3K9R2F-GP

465.0GA01.M001

緯創資通		Wistron Corporation	
RT3662A CPUCORE		ROSA NB STD POWER	
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Custom			
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OFFPAGE\_GAP



TDC=13A  
Imax=17A

NB : 330uF /9mohm\* 2pcs+22uF \* 12pcs



TBD



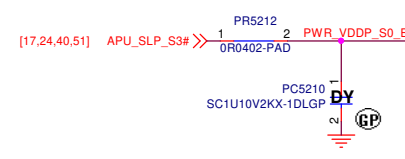
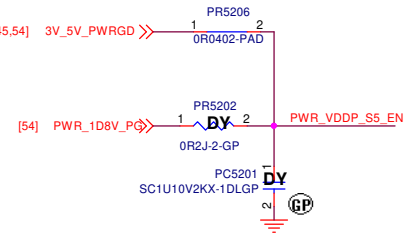
TBD



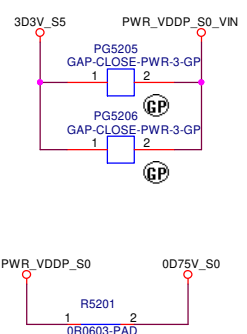
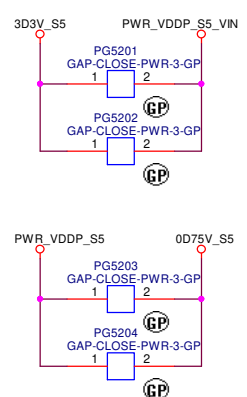




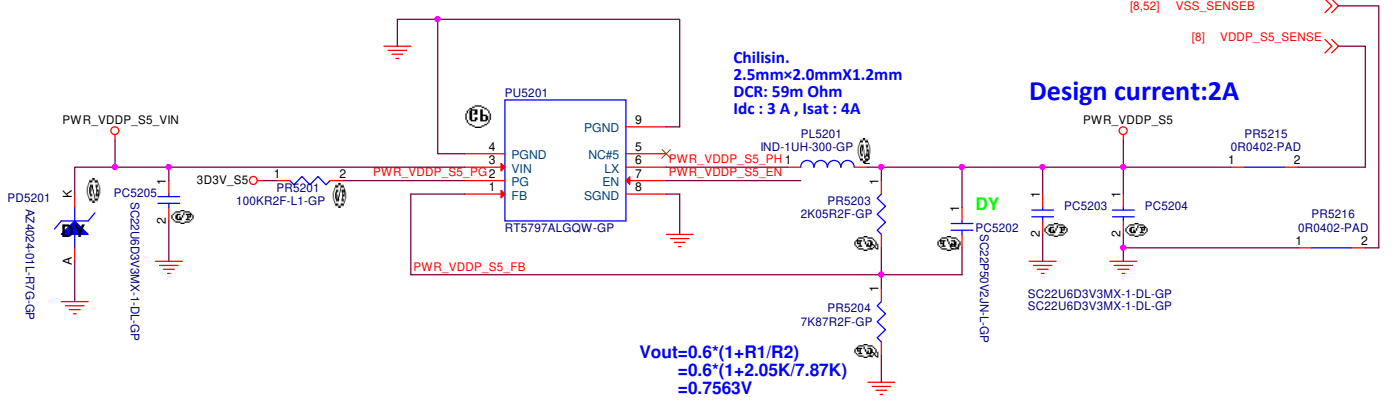
OFFPAGE-Signal



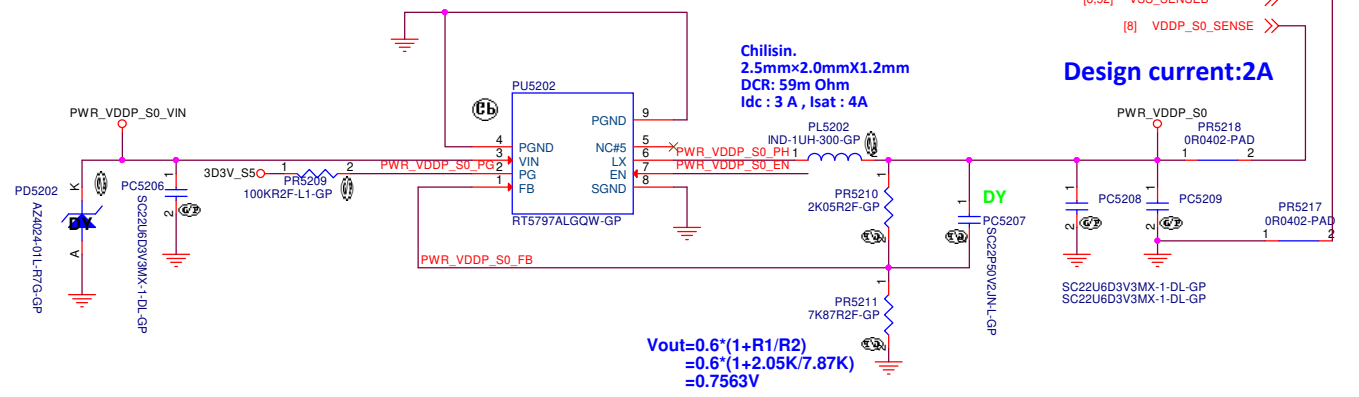
OFFPAGE-GAP



VDDP\_S5



VDDP\_S0






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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size A4	Document Number <b>Watchmen/Cyborg AMD</b>		Rev <b>X00</b>
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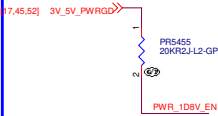
SSID = PWR.Plane.Regulator\_1D8V

OFFPAGE-Signal

PH on EE Side

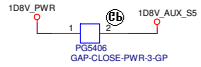
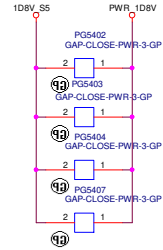
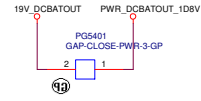
[52] PWR\_1D8V\_PG << PWR\_1D8V\_PG

20180430 follow starload

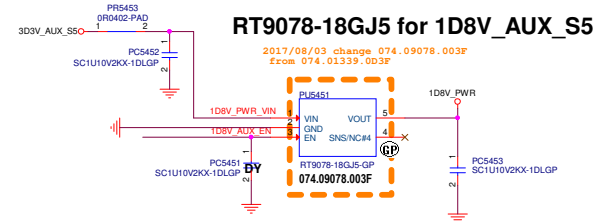
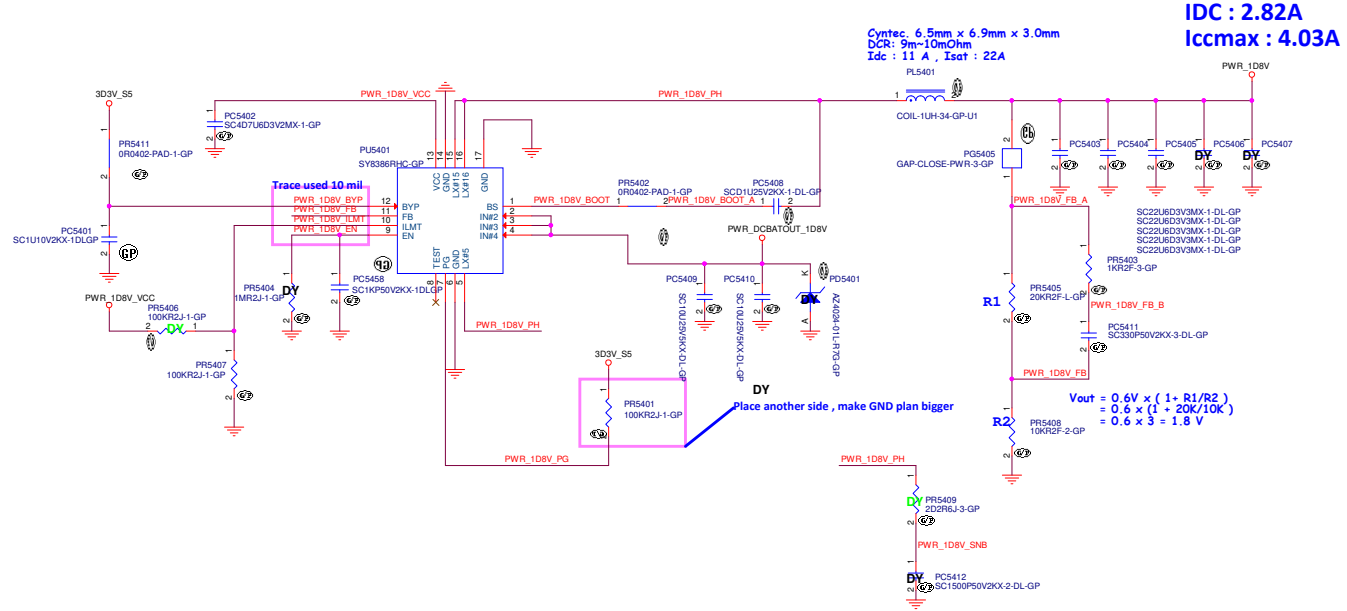


[24] 1D8V\_AUX\_EN <<

OFFPAGE-GAP



# SY8386RHC for 1D8V\_VDD



<Core Design>

<b>DELL</b> Wistron Corporation 21F, 8R, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipai Hsien 321, Taiwan, R.O.C.			
POWER (SY8386RHC_1D8V)			
Size	Document Number	Rev	
Custom	Watchmen/Cyborg AMD	X00	
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<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.3, Hsin Tai Wu Rd., Hachen, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CRT</b>			
Size A2	Document Number <b>Watchmen/Cyborg AMD</b>		Rev <b>X00</b>
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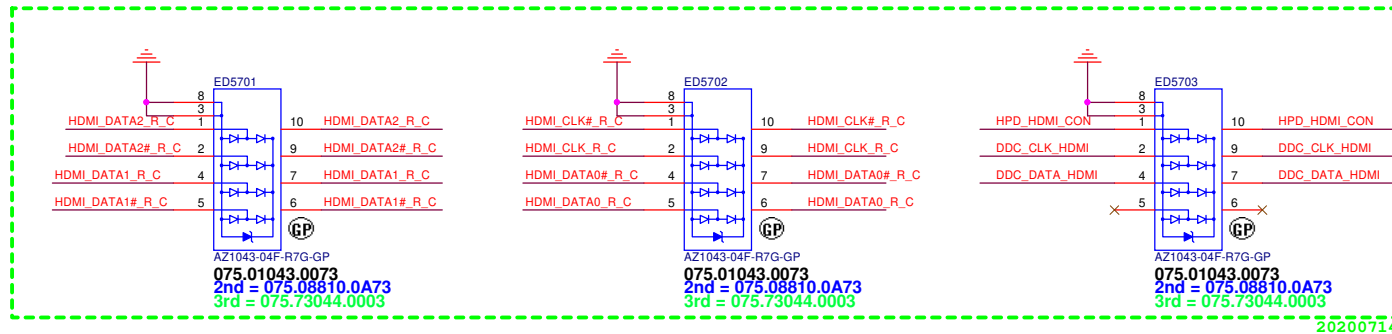
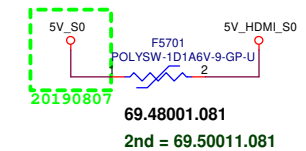
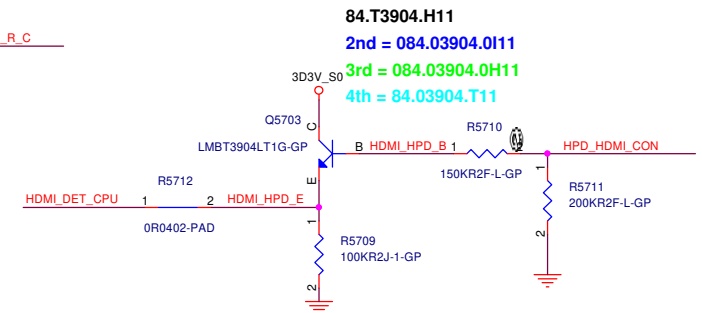
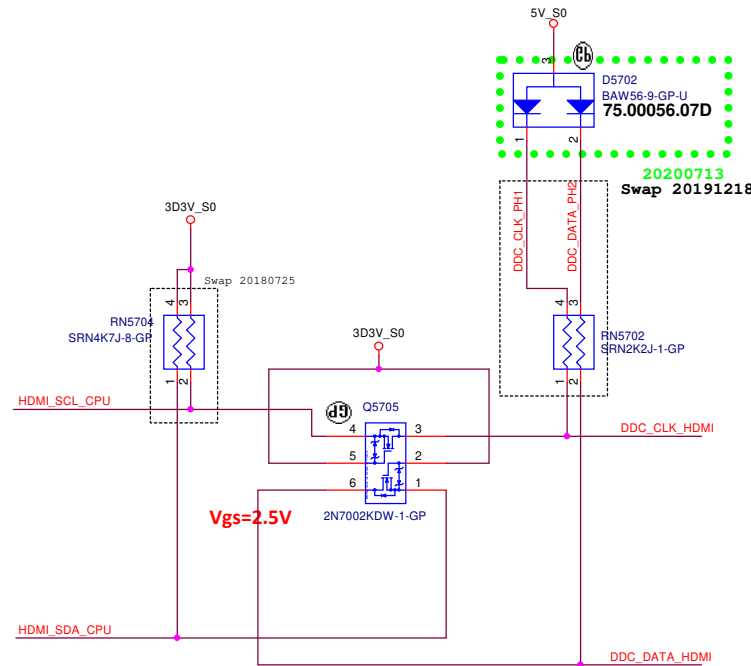
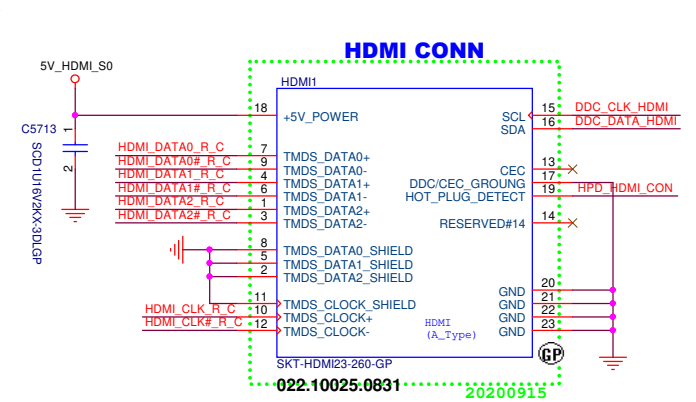
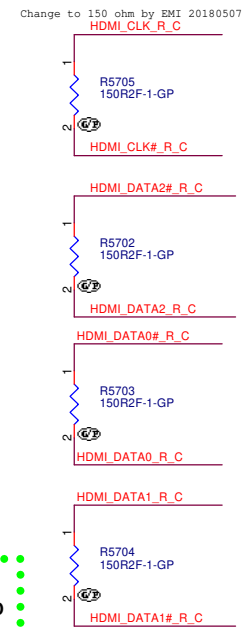
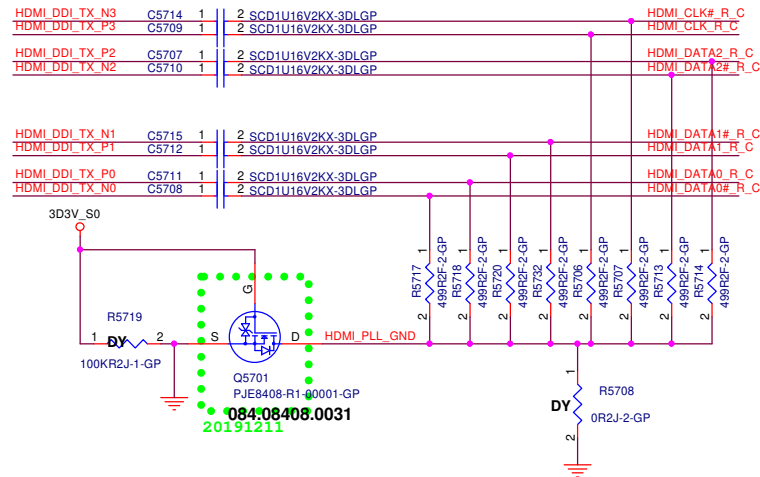
## Main Func = HDMI

[8]	HDMI_DDI_TX_N0	
[8]	HDMI_DDI_TX_P0	
[8]	HDMI_DDI_TX_N1	
[8]	HDMI_DDI_TX_P1	
[8]	HDMI_DDI_TX_N2	
[8]	HDMI_DDI_TX_P2	
[8]	HDMI_DDI_TX_N3	
[8]	HDMI_DDI_TX_P3	

[8] HDMI\_DET\_CPU <<————

[8] HDMI\_SCL\_CPU >> \_\_\_\_\_


[8] HDMI\_SDA\_CPU <>\_\_\_\_\_





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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

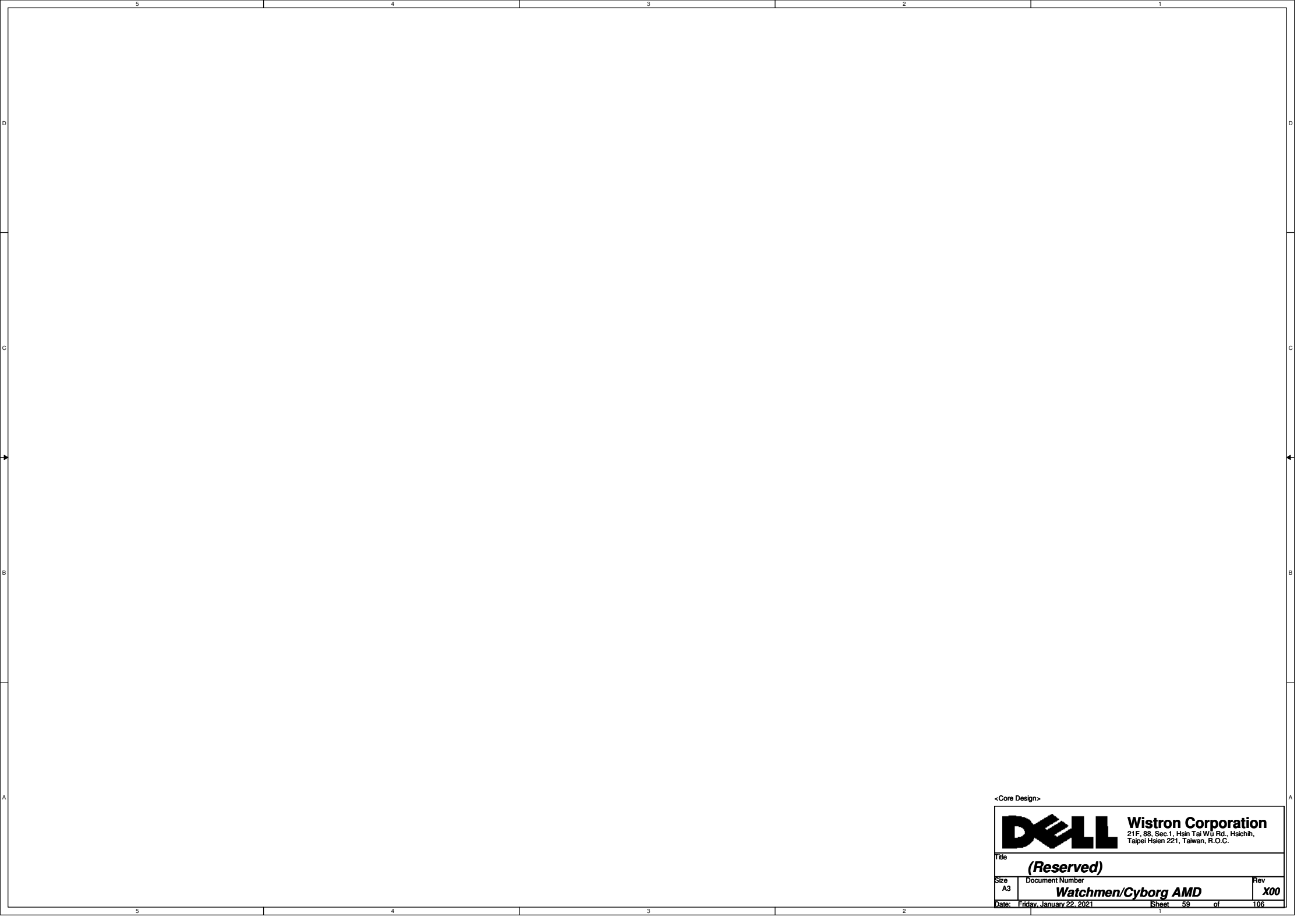
Title

**(Reserved)**

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.


Title		
<b>(Reserved)</b>		
Size	Document Number	Rev
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Main Func = HDD

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<Core Design>



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Title

**SATA IF HDD/ODD**

Size  
A3

Document Number  
**Watchmen/Cyborg AMD**

Date: Friday, January 22, 2021

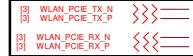
Rev  
**X00**

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# Main Func = WLAN

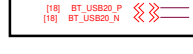
## PCIE



## PCIE\_CLK



## USB2.0



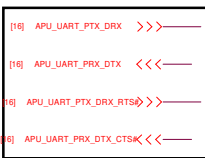
## Single end



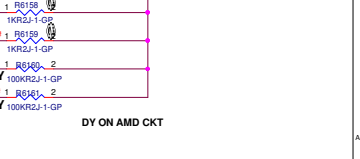
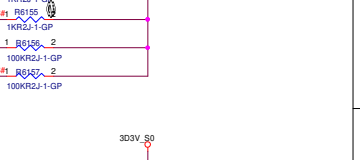
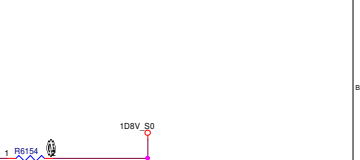
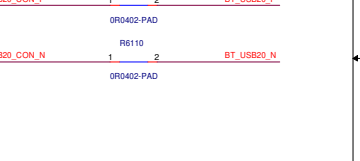
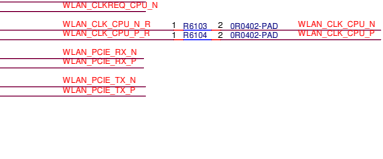
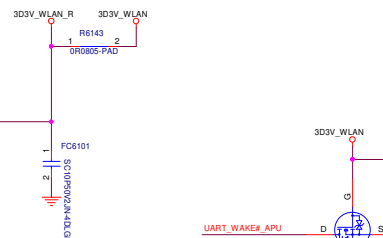
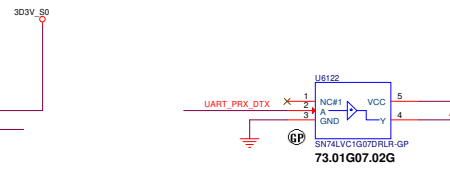
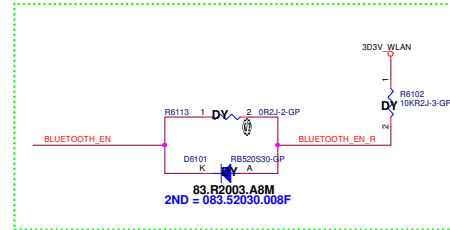
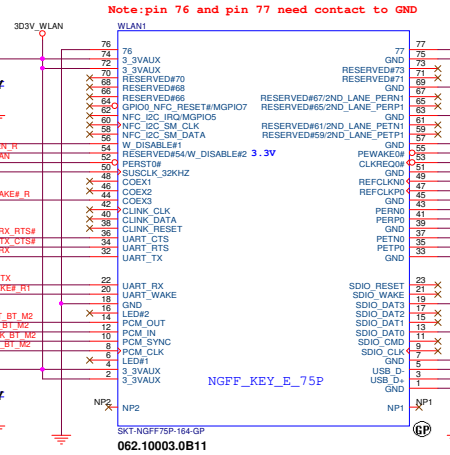
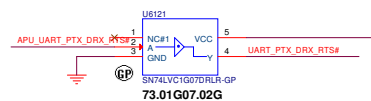
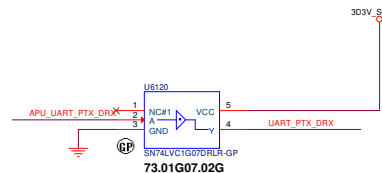
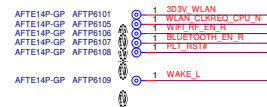
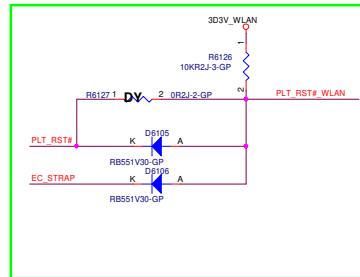
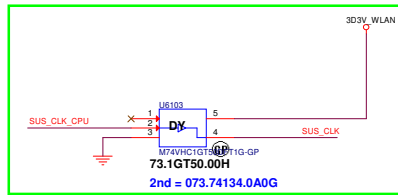
## Power EN



## UART




20190723



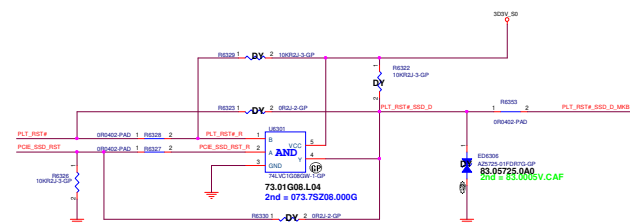
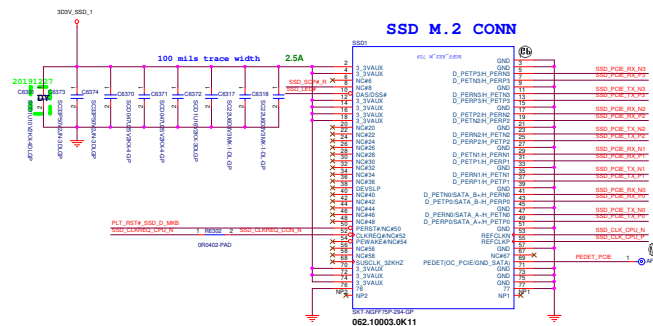


(Blanking)

<Core Design>

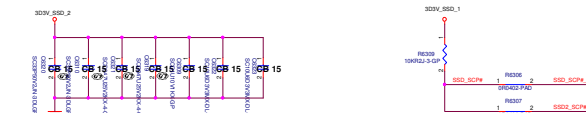
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number <b>Watchmen/Cyborg AMD</b>		Rev <b>X00</b>
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power supply	3.3V
Active Power	62mA / 0.145W SAMSUNG 65mA/0.156W Intel
Idle Power	42mA / 142mW SAMSUNG 23mA/75mW Intel

[ 5 ]	S5D_PCIE_TX_P0	>>>
	S5D_PCIE_TX_N0	>>>
	S5D_PCIE_RX_P0	>>>
	S5D_PCIE_RX_P0	>>>
[ 6 ]	S5D_PCIE_TX_P9	>>>
	S5D_PCIE_TX_N9	>>>
	S5D_PCIE_RX_P9	>>>
	S5D_PCIE_RX_N9	>>>
[ 7 ]	S5D_PCIE_TX_P10	>>>
	S5D_PCIE_TX_N10	>>>
	S5D_PCIE_RX_P10	>>>
	S5D_PCIE_RX_N10	>>>
[ 8 ]	S5D_PCIE_TX_P11	>>>
	S5D_PCIE_TX_N11	>>>
	S5D_PCIE_RX_P11	>>>
	S5D_PCIE_RX_N11	>>>
[16]	SS02_CLK_CPU_P	>>>
	SS02_CLK_CPU_N	>>>
[16]	SS02_CLKREQ_CPU_N	<<<
	[17,24,61,63,93]	P_LT_RST >>>

[illegible]



Main Func = Power BTN

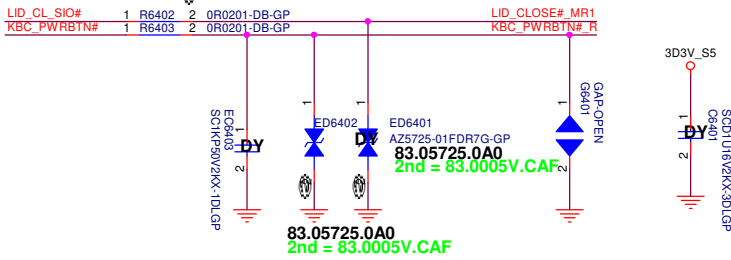
[24] LID\_CL\_SIO# <<< \_\_\_\_\_  
[24] KBC\_PWRBTN# <<< \_\_\_\_\_  
  
[67] LID\_CLOSE#\_MR1 >>> \_\_\_\_\_  
[66] KBC\_PWRBTN#\_R <<< \_\_\_\_\_

Low active from KBC GPIO

For EMI Reserved

LID\_CLOSE#\_MR1 EC6401 1 SC1KP50V2KX-1DLGP

Power button



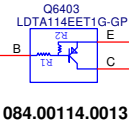
Layout note:  
G6401 place to bottom  
G6402 place to top

Main Func = Battery LED

[24] CHG\_AMBER\_LED# >>> \_\_\_\_\_  
  
[24] BATT\_WHITE\_LED# >>> \_\_\_\_\_

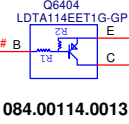
Low active from KBC GPIO

CHG\_AMBER\_LED# 1 R6405 2 CHG\_AMBER\_LED\_R# B 0R0402-PAD

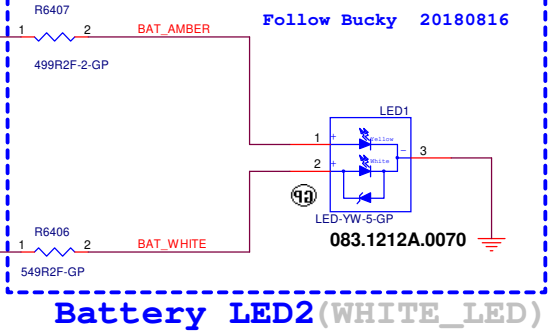


Low active from KBC GPIO

BATT\_WHITE\_LED# 1 R6404 2 BATT\_WHITE\_LED\_R# B 0R0402-PAD



Battery LED1 (AMBER\_LED)

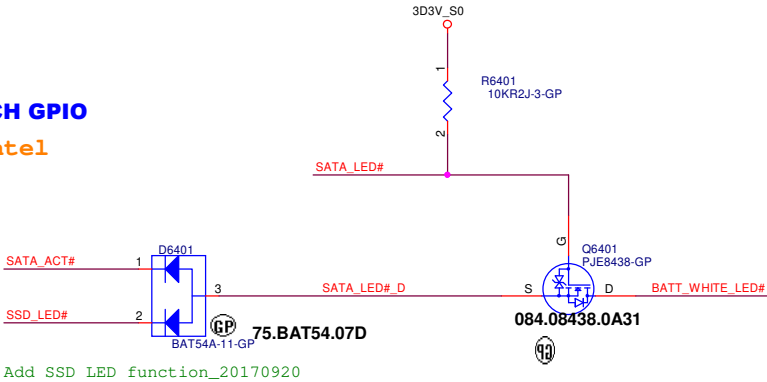


Battery LED2 (WHITE\_LED)

Main Func = HDD LED

[24] SATA\_LED# >>> \_\_\_\_\_  
  
[17] SATA\_ACT# >>> \_\_\_\_\_  
[63] SSD\_LED# >>> \_\_\_\_\_

SATA HDD LED  
LOW active from PCH GPIO  
EVT 0509 :Copy Intel



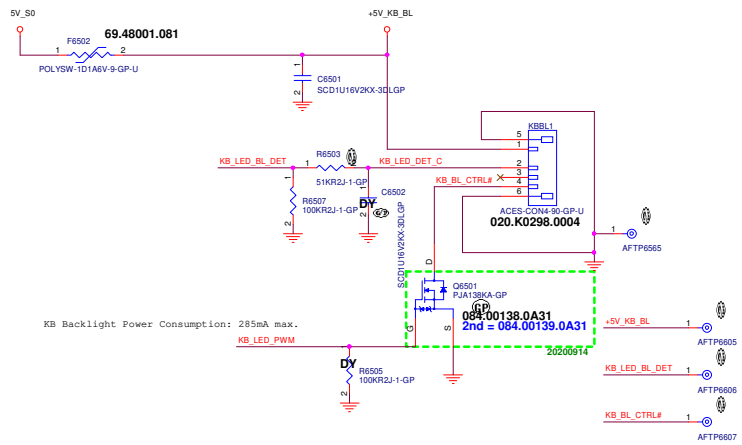
Layout note:  
G6401 place to bottom  
G6402 place to top



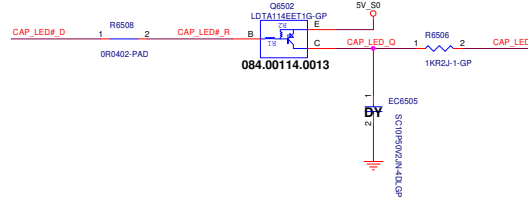
Main Func = KB

- 20180402
- [24] CAP\_LED#\_D >>> \_\_\_\_\_
- [24] KS[0..7] >>> \_\_\_\_\_
- [24] KSQ[0..16] <<< \_\_\_\_\_
- [16] KB\_DET# <<< \_\_\_\_\_
- [17] KB\_LED\_BL\_DET <<< \_\_\_\_\_
- [24] KB\_LED\_PWM >>> \_\_\_\_\_

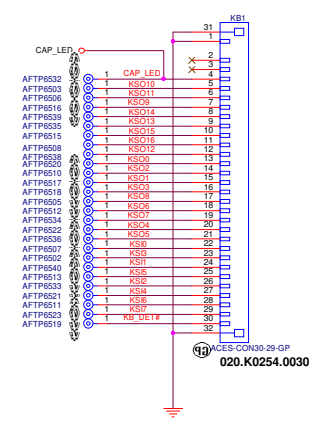
Keyboard Backlight (Reserved)



CAP LED Control  
LOW active from KBC GPIO



Internal Keyboard Connector



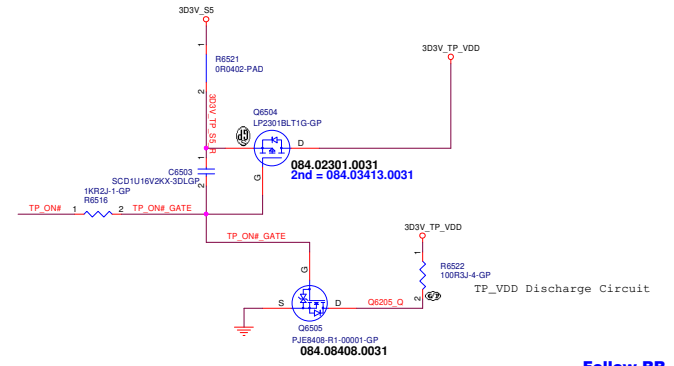
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Main Func = TPAD

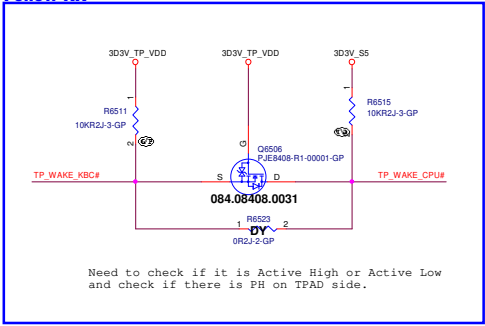
- [24] TP\_WAKE\_KBC# <<< \_\_\_\_\_
- [17] TP\_WAKE\_CPU# <<< \_\_\_\_\_
- [24] TP\_ON# >>> \_\_\_\_\_
- [24] TP\_LOCK# <<< \_\_\_\_\_
- [24] CLK\_TP\_SIO <<< \_\_\_\_\_
- [24] DAT\_TP\_SIO <<< \_\_\_\_\_
- [17.66] CPU\_IC\_SCL\_P3 >>> \_\_\_\_\_
- [17.66] CPU\_IC\_SDA\_P3 >>> \_\_\_\_\_

BOM SELECT TP\_WAKE

NO STUFF NON TP\_WAKE



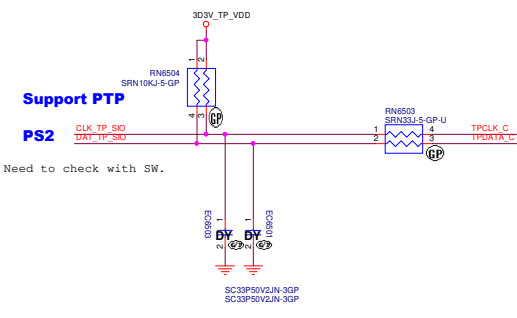
Follow RR



Support PTP

PS2

Need to check with SW.

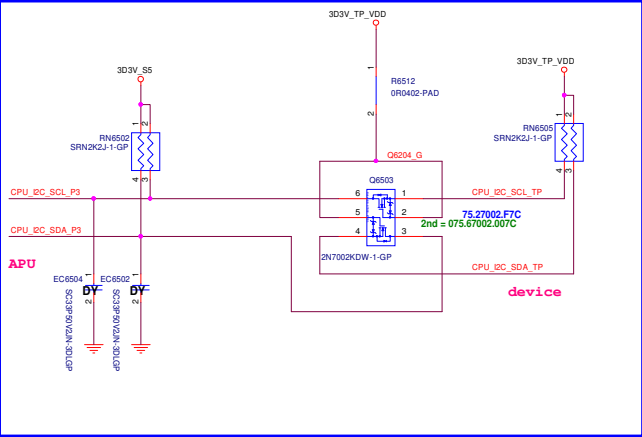


I2C

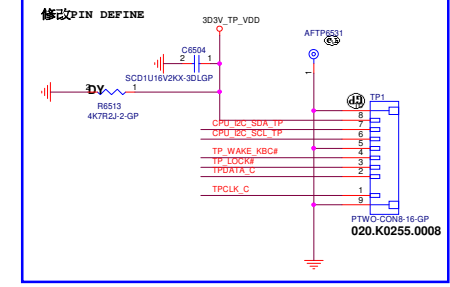
APU

device

Follow RR



Precision Touch Pad Connector



<Core Design>



**Main Func = IO Connector**

AUDIO

```
[27,29]  AUD_RING      <<< _____
[27,29]  AUD_SLEEVE    <<< _____
[29]     AUD_HP1_JACK_L1 <<< _____
[29]     AUD_HP1_JACK_R1 <<< _____
[27]     AUD_SENSE      >>> _____
```

## CRD

```
[18] CARD1_USB20_N <<>>=====
[18] CARD1_USB20_P <<>>=====
```

USB3.0

**PORT1**

[18]	USB2_USB30_RX_N	}}	}}	_____
[18]	USB2_USB30_RX_P	}}	}}	_____
[18]	USB2_USB30_TX_N	}}	}}	_____
[18]	USB2_USB30_TX_P	}}	}}	_____
[18]	USB2_USB20_N	}}	}}	_____
[18]	USB2_USB20_P	}}	}}	_____
[24]	KB_CLOSE#_2	<<<		_____

**I2C**

[17,65] CPU\_I2C\_SCL\_P3 >>> \_\_\_\_\_  
[17,65] CPU\_I2C\_SDA\_P3 <<< \_\_\_\_\_

## LAN

```

[3] LAN_PCIE_RX_N >>>
[3] LAN_PCIE_RX_P >>>
[3] LAN_PCIE_TX_N >>>
[3] LAN_PCIE_TX_P >>>

[16] LAN_CLK_CPU_N <<<
[16] LAN_CLK_CPU_P <<<

[16] LAN_CLKREQ_CPU_N >>>

[24] PM_LAN_ENABLE >>>

[24] PCIE_LAN_WAKE# >>>

```

## FP

```

[18] FP1_USB20_N  <<<<-----
[18] FP1_USB20_P  <<<<-----

[24] FPR_SCAN#    >>>-----

[24,64] LID_CL_SIO# <<<-----

[64] KBC_PWRBTN# R >>>-----

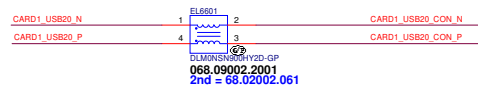
```

```
[17,24,51]  APU_SLP_SS#  >>>=====
[24]  PLT_RST#_LAN  <<<=====
[44]  PWR_CHG_VBATIN  >>>=====
4,61,63,91]  PLT_RST#  <<<=====
[67]  LID_C1_NB#  >>>>=====
```

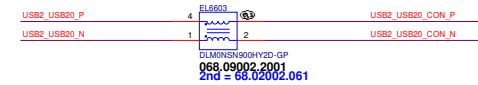
4,61,63,91] PLT\_RST# <<< \_\_\_\_\_  
[67] LID\_C1\_NB# >>> \_\_\_\_\_

[67] LID\_C1\_NB# >>> \_\_\_\_\_

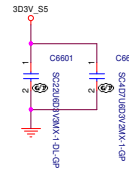
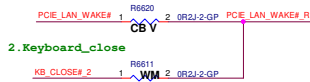
## CRD



USB3.0 PORT2



**FPR**



### I/O Board Connector (Colay)

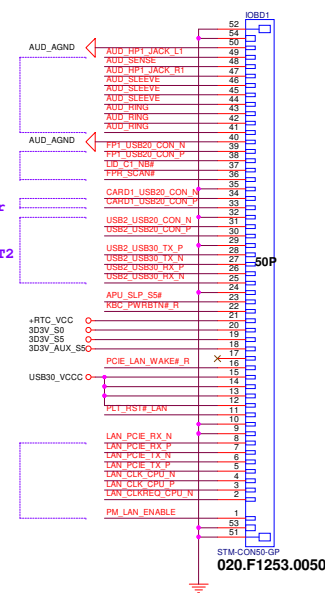


FINGER  
PRINTER

### Card Reader

USB3.1 PORT2

## LAN

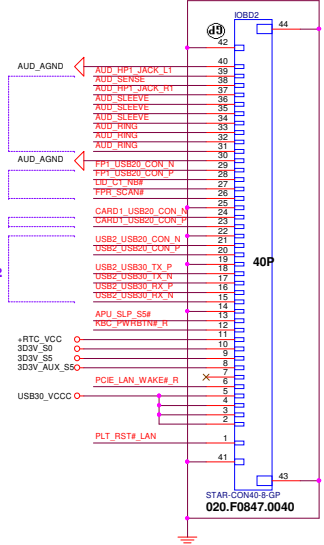


## AUDIO

FINGER  
PRINTER

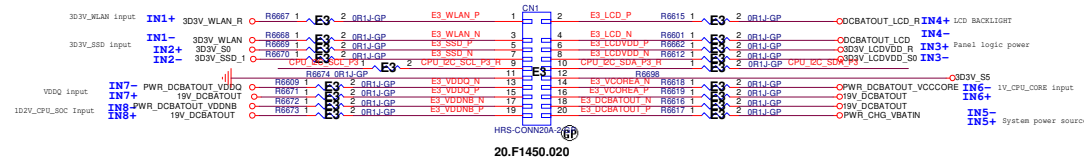
### Card Reader

## USB3.1 PORT2



# E3

**4mil for trace width and trace to trace .**



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Title			
<b>IO Board Connector</b>			
Size A2	Document Number	Rev	
	<b>Watchmen/Cyborg AMD</b>	<b>X00</b>	
Date:	Friday, January 22, 2021	Sheet 66 of	106

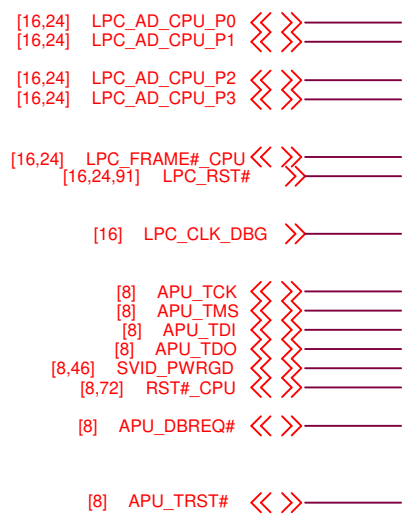


## Main Func = Hall Sensor



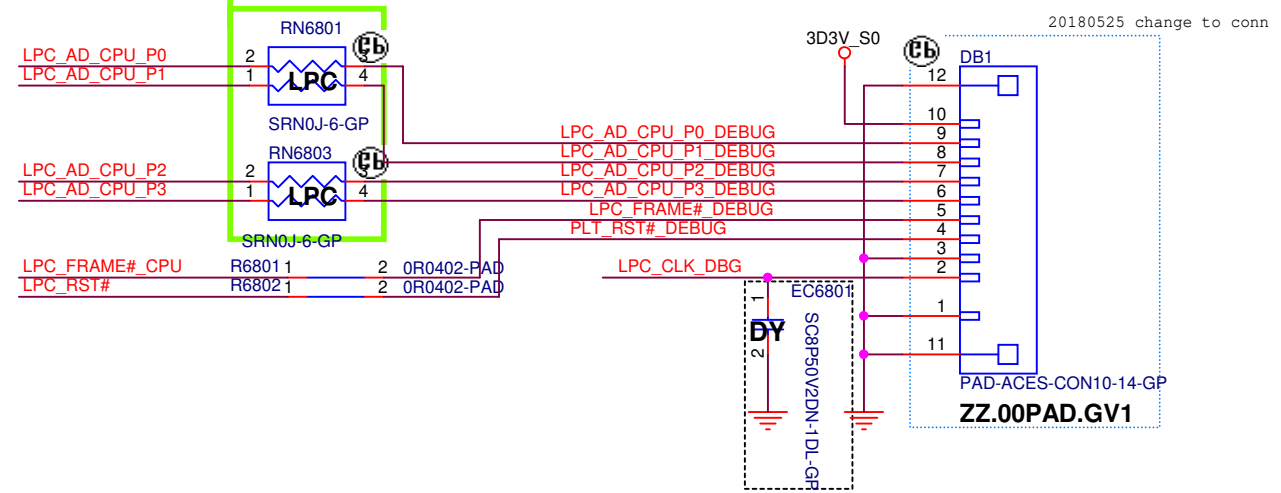


SSID = DEBUG PORT



**Layout Note:**  
Place near trace separated point.

**Debug Connector**

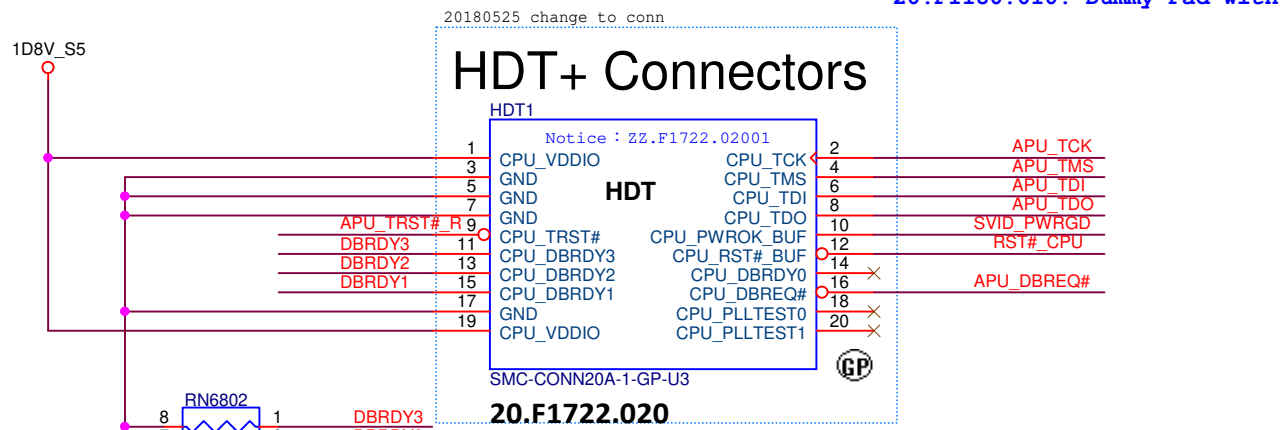


RF request 2017/11/08 modify

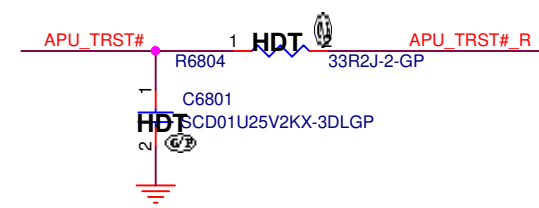
20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41

DB1 Optional: New one smaller LPC connector is 20.F1180.010.

20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1



20.F1722.020: Dummy Pad with solder mask is ZZ.F1722.02001



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Title **Dubug connector**

Size A4 Document Number **Watchmen/Cyborg AMD** Rev **X00**

Date: Friday, January 22, 2021 Sheet 68 of 106

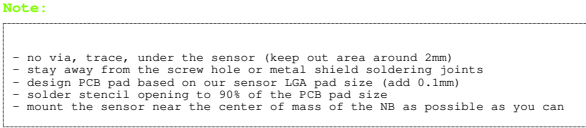


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## Mantis Accelerometer for adaptive thermal and HDD protection

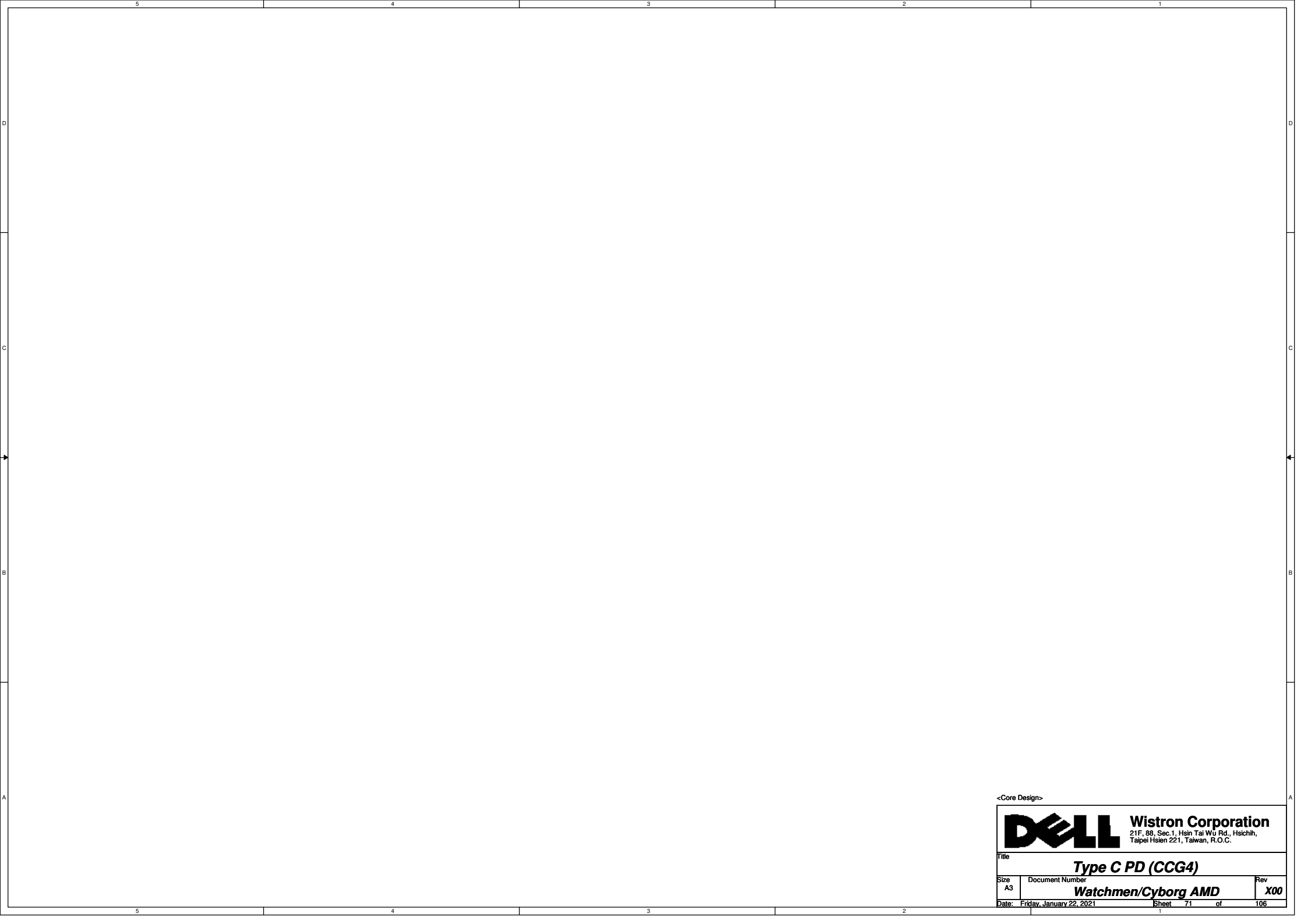
The slave address (SAD) associated to the **LNG2DM** is **010100xb**. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I<sup>2</sup>C lines.




**Note:**

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.





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Title			
<b>Type C PD (CCG4)</b>			
Size	Document Number		Rev
A3	<b>Watchmen/Cyborg AMD</b>		<b>X00</b>
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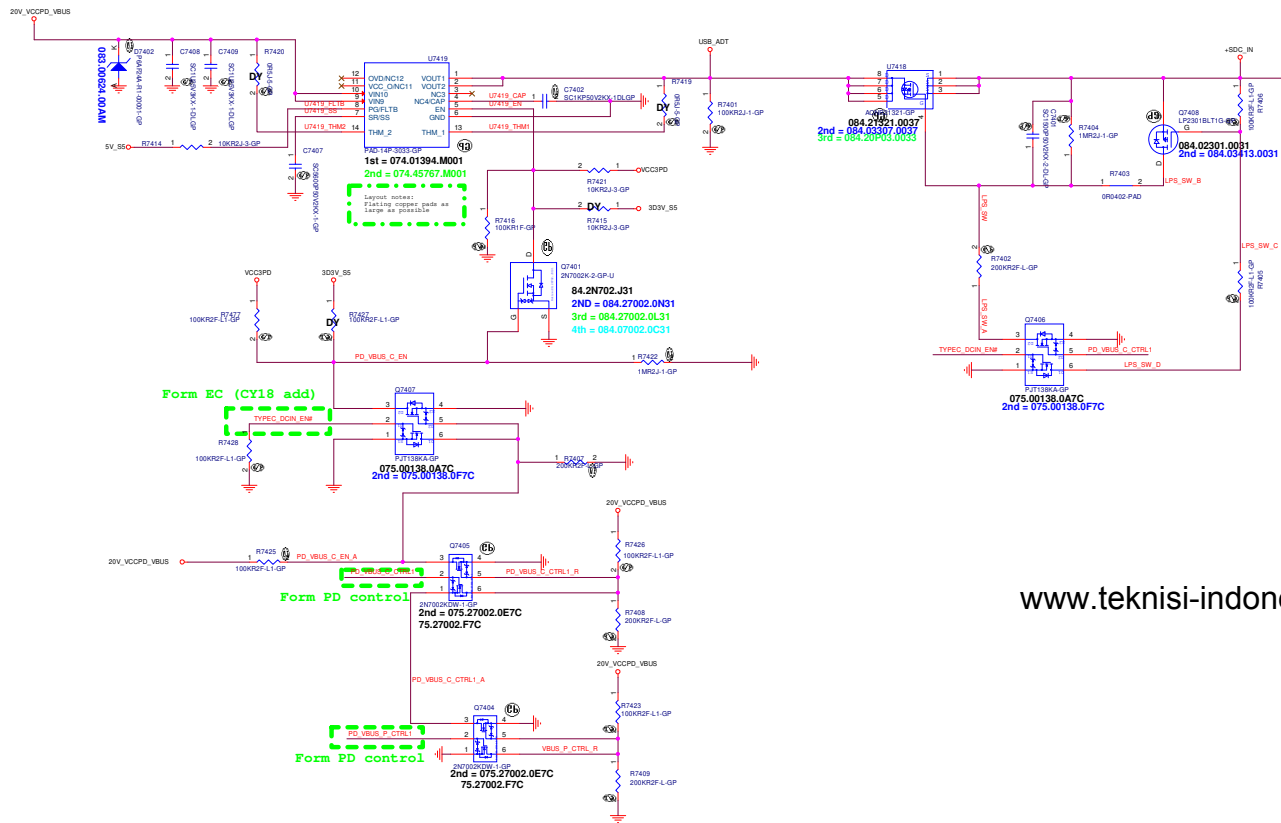








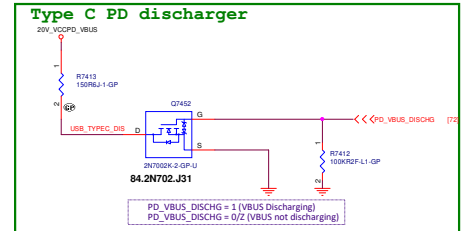
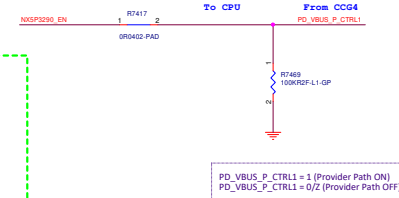
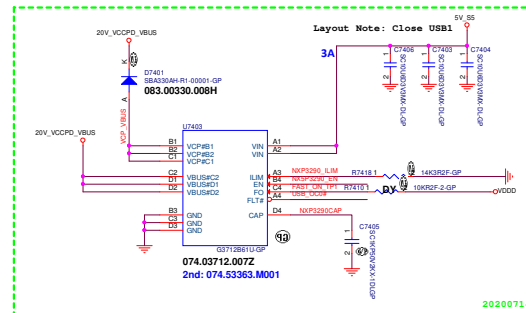
[72] PD\_VBUS\_P\_CTRL1 >>>  
 [73] PD\_VBUS\_C\_CTRL1 >>>  
 [84] TYPEC\_DCN\_ENW >>>  
 [44] U7419\_FLTB >>>  
 [72,74] FAST\_ON\_TPH >>>  
 [18,74] USB\_OCIN <<<



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Fast turn on Detect Pin(REMOVE)

current-limited power switch




[72,74] FAST\_ON\_TPH >>> FAST\_ON\_TPH  
 [18,74] USB\_OCIN >>> USB\_OCIN

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Size  
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Main Func = dGPU

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Title

**GPU (1/5) PEG**

Size  
A3

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<b>GPU (2/5) DIGITALOUT</b>			
Size	Document Number	Rev	
Custom	<b>Watchmen/Cyborg AMD</b>	<b>X00</b>	
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		<b>Wistron Corporation</b> 21F, B2, Sec.1, Hsin Tai Wu Rd., Heichah, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU (2/5) DIGITALOUT</b>			
Size	Document Number		Rev
Custom	<b>Watchmen/Cyborg AMD</b>		<b>X00</b>
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Title

GPU (3/5) VRAM I/F

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Title		
GPU (5/5) PWR/GND		
Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00
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<Core Design>		
		<b>Wistron Corporation</b> <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>
Title <b>GPU VRAM1,2 (1/4)</b>		
Size C	Document Number <b>Watchmen/Cyborg AMD</b>	Rev <b>X00</b>
Date: Friday, January 22, 2021		
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File  
GPU (BOMACO)

Size  
C

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Rev  
X00

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Main Func = dGPU


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Main Func = dGPU

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Title

**GPU-VRAM7,8 (4/4)**

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Friday, January 24, 2025

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X100



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Title					
<b>GPU DISCHARGE</b>					
Size	Document Number				Rev
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X00

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[16,24,68]	LPC_RST#	>>>	_____
[17,24,61,63]	PLT_RST#	>>>	_____
[24,25]	SPI_CLK_ROM_R	>>>	_____
[16,24,25]	SPI_SI_ROM	>>>	_____
[16,24,25]	SPI_SO_ROM	>>>	_____
[16]	SPI_CS_ROM_N2	>>>	_____
[17]	PIRQA#	>>>	_____
[24]	KBC_TPM_RST#	>>>	_____



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Title
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### ***INT IO (TPM)***

Size  
A4

Document Number
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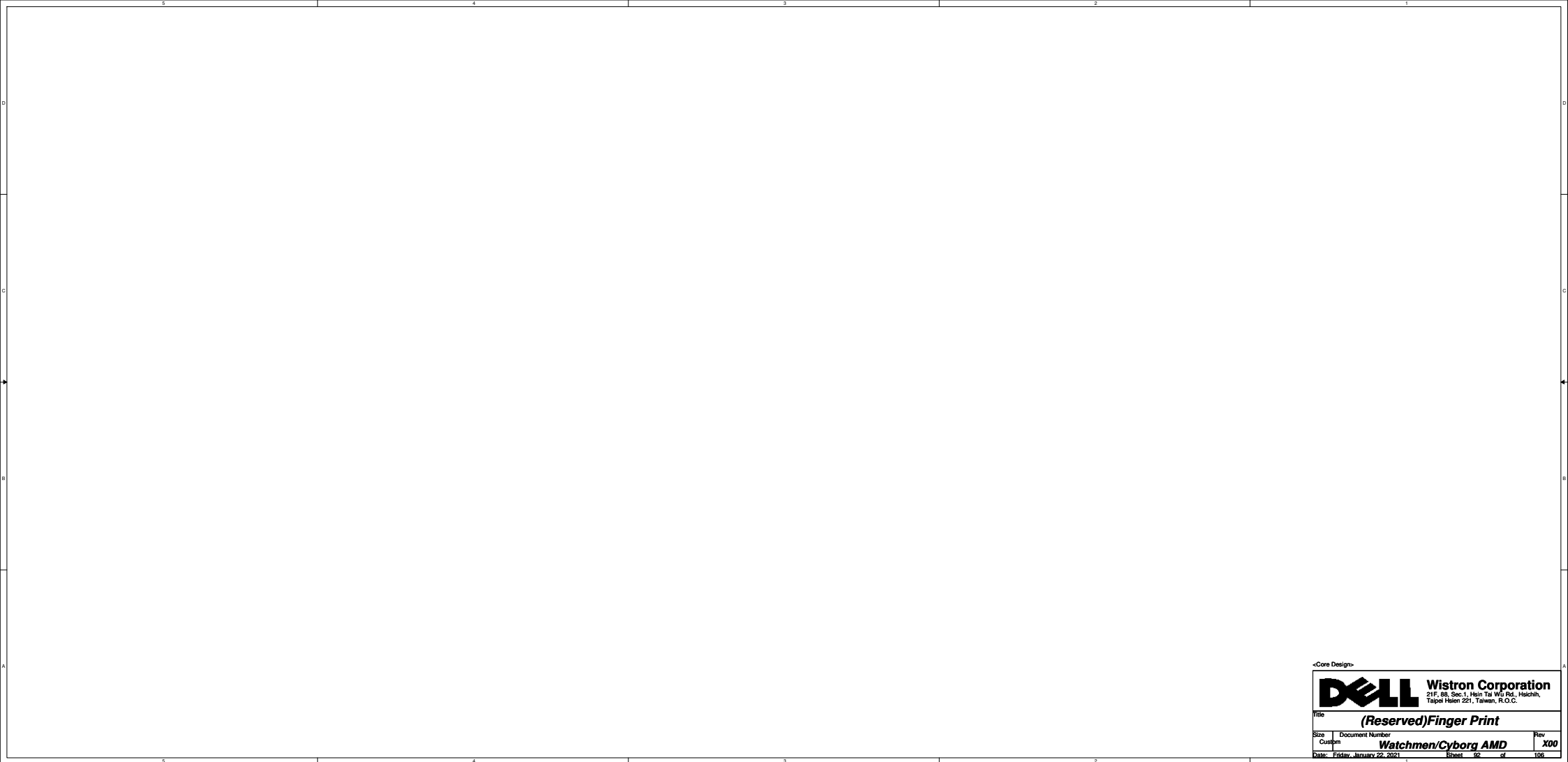
### **Watchmen/Cyborg AMD**

Rev  
Y00

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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taippei Hsien 221, Taiwan, R.O.C.	
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Size Custom	Document Number <b>Watchmen/Cyborg AMD</b>		Rev <b>X00</b>
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Title

**LVDS Switch**


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CRT Switch

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Main Func = Debug

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***CPU XDP;PCH XDP***

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Title			
<b>CLK Block Diagram</b>			
Size	Document Number	Rev	
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# Change notes -

Phase	Date	Sch Page	Location	Reason of change	Owner
DVT1	2018/9/13	24	Add D2409 ,R2489 to KBC_GPI005 for Mods about Lan function.	Follow AMD's suggestion	EE
DVT1	2018/9/18	16	R1623/R1624 OR 0402->0201	Add layout spacing	EE
DVT1	2018/9/20	40	ADD R4014	For break down easily	EE
DVT1	2018/9/20	30	R4637 change to 340 ohm,PR4601 change to 187 ohm, and PR4601 change to 187 ohm	Follow AMD's stardust test result	PWR
DVT1	2018/9/21	46	PR4625 change 9.53K/0402 for VR HOT	For VR HOT	PWR
DVT1	2018/9/21	16	R1609 change 33ohm and EC1615 change 33P	Reduce noise	EMC
DVT1	2018/9/27	24	R2428	20K for PCB_VERSION_DVT1	EE
DVT2	2019/11/13	44,48	TC4801 PT4402	DY by acoustic test	EE
DVT2	2019/11/15	24	R2428	33K for PCB_VERSION_DVT2	EE
DVT2	2019/11/16	74	C7493 DY,C7491 C7492 10U change to 22U	Follow Factory suggestion	EE
A00	2018/12/3	8	R806,R807,R809	short PAD for MP	EE
A00	2018/12/3	9	R901,R902,R903,R904	short PAD for MP	EE
A00	2018/12/5	11	R1102,R1103,R1104,R1105,R1106	short PAD for MP	EE
A00	2018/12/5	16	R1613,R1614,R1621,R1622,R1607,R1616	short PAD for MP	EE
A00	2018/12/7	17	R1772,R1722,R1723,R1773,R1712,R1706	short PAD for MP	EE
A00	2018/12/21	18	R1807	short PAD for MP	EE
A00	2018/12/21	24	R2411,R2416,R2419,R2420,R2413,R2445,R2468,R2422,R2457,R2456,R2421,R2426,R2427,R2437,R2443	short PAD for MP	EE
A00	2018/12/21	24	R2428	47K for PCB_VERSION_A00	EE
A00	2018/12/21	25	R2508	short PAD for MP	EE
A00	2018/12/21	26	R2618,R2619,R2615,R2605,R2613,R2614,R2612	short PAD for MP	EE
A00	2018/12/24	27	R2741,R2734,R2721,R2718,R2712,R2720,R2704,R2705,R2706,R2708	short PAD for MP	EE
A00	2018/12/24	29	R2901,R2902,R2903,R2904,R2906,R2907,R2909,R2911,R2923,R2914	short PAD for MP	EE
A00	2018/12/24	34	R3432	short PAD for MP	EE
A00	2018/12/24	35	R3501,R3502,R3503,R3504,R3512,R3524,R3533,R3521,R3522	short PAD for MP	EE
A00	2018/12/24	38	R3805,R3806,R3821,R3822,R3803	short PAD for MP	EE
A00	2018/12/25	40	R4001,R4013,R4012,R4008,R4007,R4005	short PAD for MP	EE
A00	2018/12/25	40	R4014	remove R4014,short	EE
A00	2018/12/25	43	EL4301,EL4302,EL4303,EL4304,R4380	short PAD for MP	EE
A00	2018/12/25	55	R5514,R5523,R5508,R5531,R5502,R5537,R5538	short PAD for MP	EE
A00	2018/12/25	57	R5712,R5715	short PAD for MP	EE
A00	2018/12/25	60	R6001,R6016	short PAD for MP	EE
A00	2018/12/25	61	R6143,R6110,R6111	short PAD for MP	EE
A00	2018/12/25	63	R6328,R6327	short PAD for MP	EE
A00	2018/12/25	63	R6321,R6331	改成兩個 0805 Short PAD	EE
A00	2018/12/25	64	R6404,R6405	short PAD for MP	EE

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## Change History

Size

A3 Document Number

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Rev

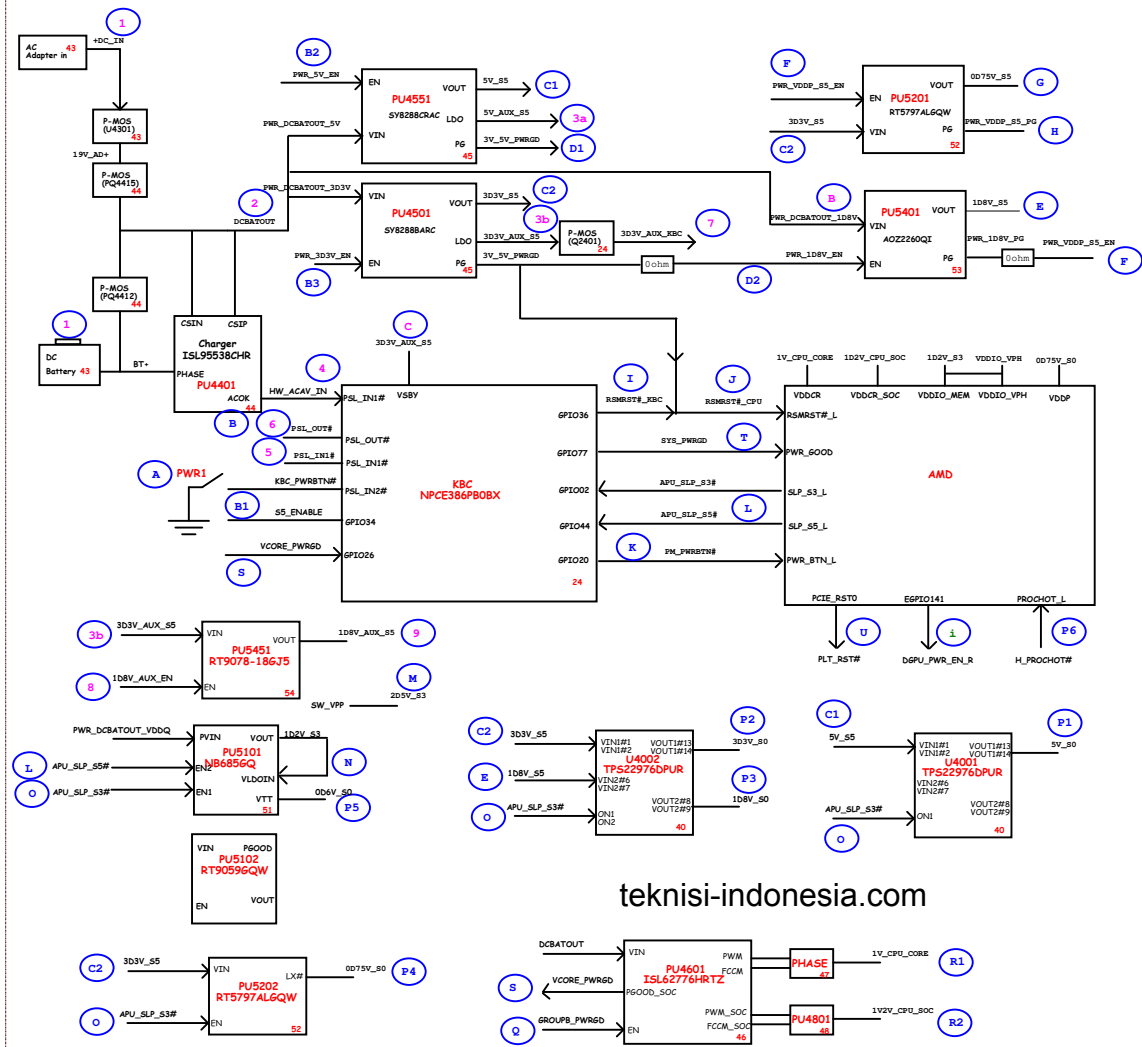
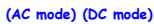
**X00**

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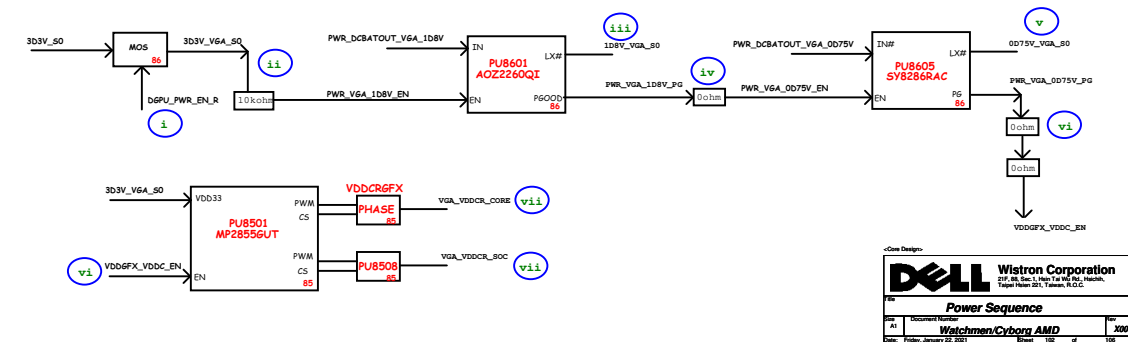
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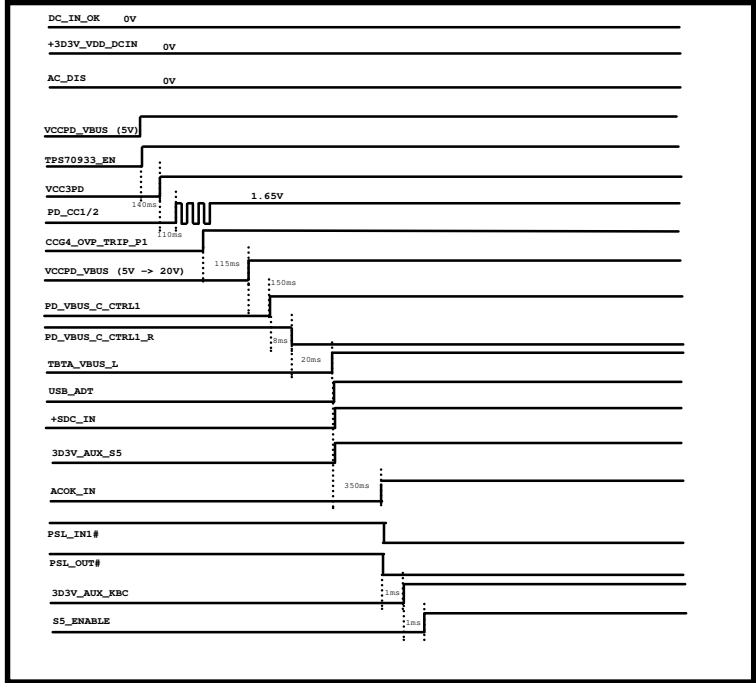




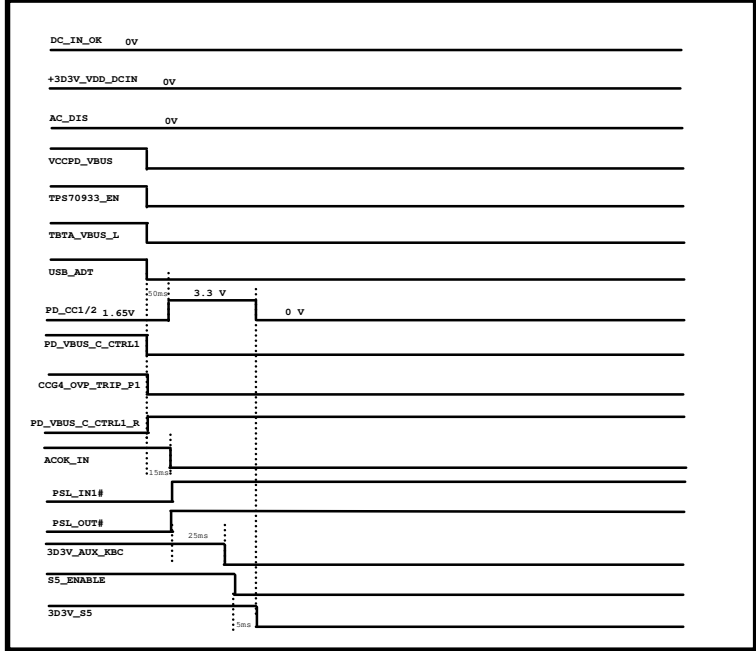


# Type-C Adapter sequence

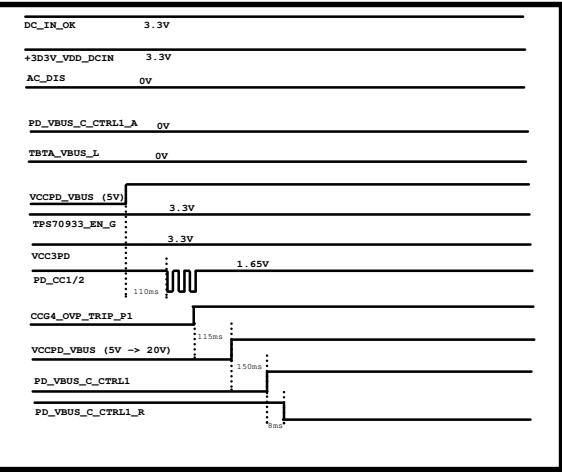
## Type-C ADP IN without Barrel ADP (DC mode)



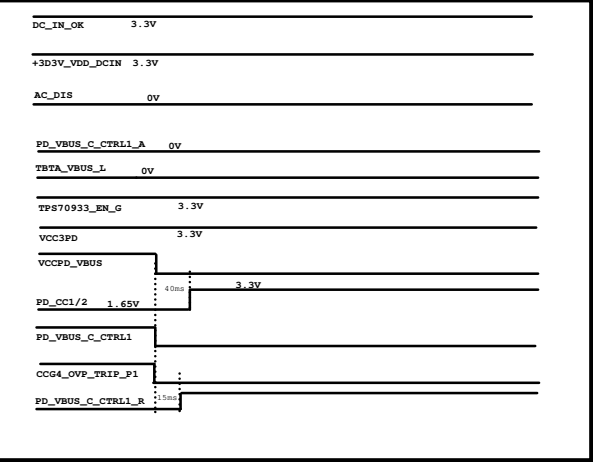
## Type-C ADP OUT without Barrel ADP (DC mode)



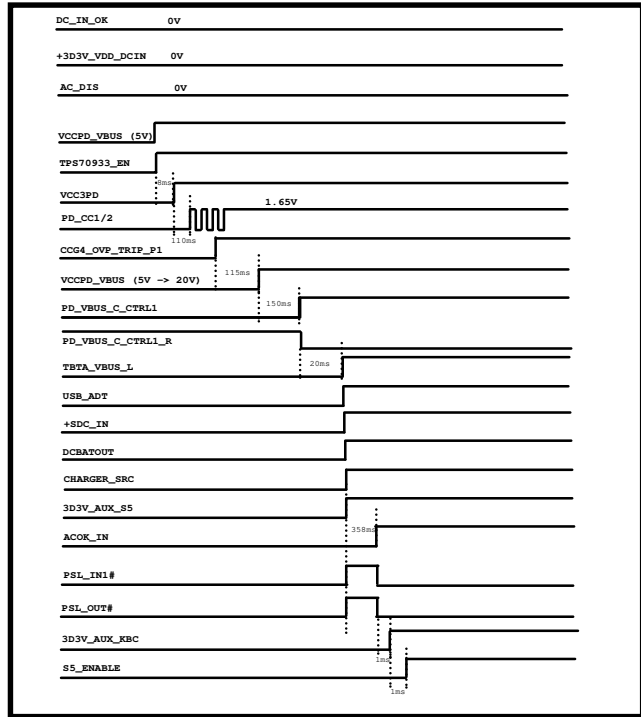
## Type-C ADP IN after Barrel ADP in



## Type-C ADP OUT after Barrel ADP in

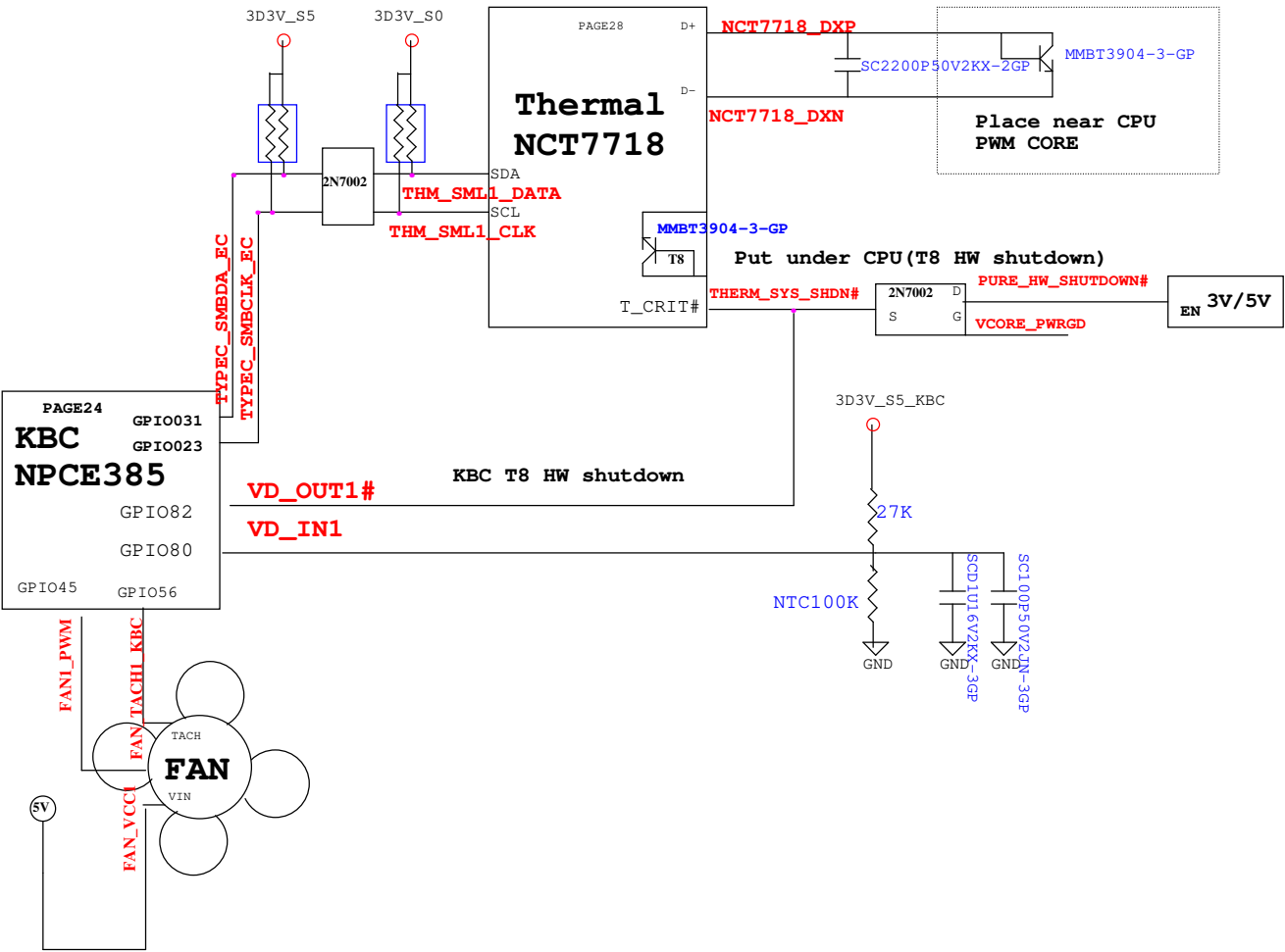


## Type-C ADP IN without battery (Dead Battery)

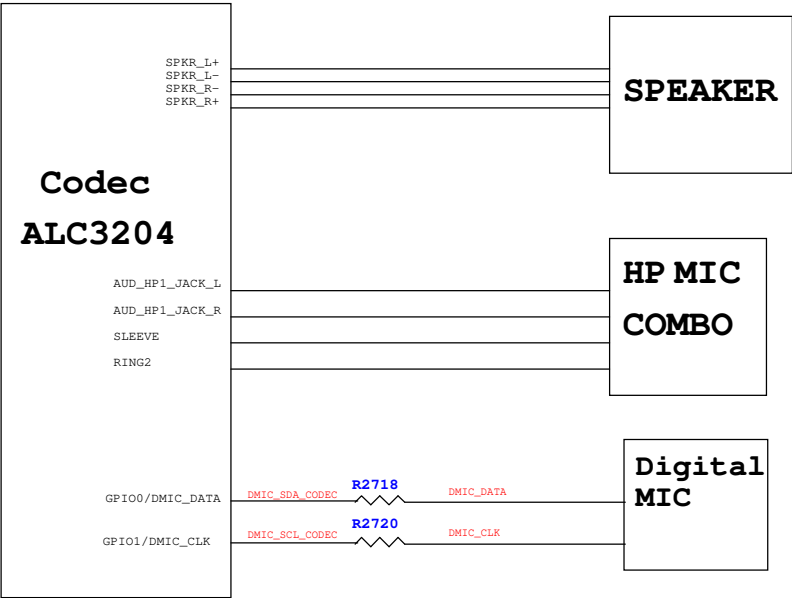




# Thermal Block Diagram



# Audio Block Diagram





CLK Block Diagram

